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Effects of p-GaN Capping Layer on the Current Collapse Behaviors in Normally-off p-GaN Gate AlGaN/GaN HFETs

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1. Introduction

Recently, AlGaN/GaN heterostructure field effect transistors (HFETs) with a p-GaN gate stack was proposed to convert the AlGaN/GaN HFETs into normally-off devices [1]. A p-GaN barrier below the gate depletes the channel and increases the turn on voltage larger than 0V. Although, the p-GaN gate structure can make the AlGaN/GaN HFETs attractive for high-power applications by combining the high-mobility 2-DEG transistor channel with a secure normally-off operation, the current collapse effects related with surface and/or bulk traps are still critical problems which need to be overcome for the successful commercialization of AlGaN/GaN HFETs [2]. For a high-voltage AlGaN/GaN HFET working at a switching mode, the current collapse effect always results in dynamic performance degradation, i.e., longer switch on delay time and higher dynamic ON-state resistance (R_{ON}), which increases the power consumption in the electrical energy conversion systems. In this work, we investigate the effects of p-GaN capping layer on the current collapse behaviors in normally-off p-GaN gate AlGaN/GaN HFETs. From the experimental results, it was shown that the p-GaN capping layer can act as an effective passivation layer in p-GaN gate AlGaN/GaN HFETs.

2. Device Fabrication

Figure 1 depicts the schematic of the fabricated p-GaN gate AlGaN/GaN HFETs with a p-GaN capping layer. The material structure for the fabricated device is consisted of a 3 μm-thick GaN, a 30 nm-thick AlGaN, and a 100 nm-thick Mg-doped p-GaN gate layer grown on a Si (111) substrate. The capping layer was formed by leaving a thin p-GaN layer on the gate-to-drain/source access regions without a complete etching of the p-GaN layer. For the source and drain contacts, ohmic metal was deposited by e-beam evaporation, patterned by a lift-off process, and annealed by rapid thermal annealing (RTA) process. The gate metal was deposited by e-beam evaporation and was patterned by a lift-off process.

3. Results and Discussions

Figure 2 shows the drain current (I_D) and gate current (I_G) versus the gate-to-source voltage (V_{GS}) measured for p-GaN gate AlGaN/GaN HFETs with and without a p-GaN capping layer, respectively. The devices were measured at a drain-to-source voltage (V_{DS}) of 0.5 V. It shows that the turn-on voltages of both devices are ~ 1.3 V, and there is no

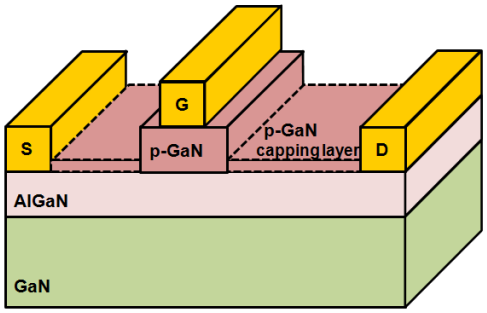

Fig. 1 Schematic of the fabricated p-GaN gate AlGaN/GaN HFETs with a p-GaN capping layer.

significant difference in on-current and gate leakage current between the devices without and with a p-GaN capping layer. Previous researches have shown that the high-k dielectric-based passivation layer can cause the negative turn-on voltage shift in AlGaN/GaN HFETs [3]. Such a phenomenon was not observed in devices with a p-GaN capping layer in our experiments.

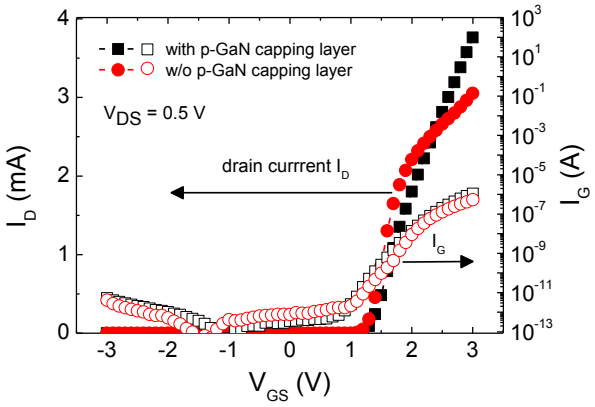

Fig. 2 I_D *and* I_G *versus* V_{GS} measured for p-GaN gate AlGaN/GaN HFETs with and without a p-GaN capping layer.

We have employed the gate lag measurements on the devices with and without a p-GaN capping layer to investigate the surface passivation effects of the p-GaN capping layer. Figure 3(a) and (b) show the normalized I_Ds as a function of V_{GS} for both DC and pulsed measurements in devices without and with a p-GaN capping layer, respectively. Pulse widths of 1 and 100 μs (duty ratio 10 %) were used in the measurements, and V_{GS} is switched from -3 V to the values shown on the x-axis. The large differences be-

tween the DC and pulsed I_D in the devices without a p-GaN capping layer can be attributed to the surface traps in the gate-to-drain access region. The device with a p-GaN capping layer exhibits a marked increase in the pulsed I_D, which represents that a p-GaN capping layer can effectively reduce the surface trapping effects.

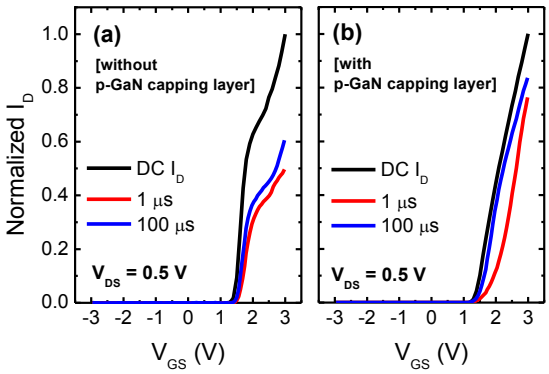

Fig. 3 Normalized I_Ds as a function of V_{GS} for both DC and pulsed measurements in devices (a) without and (b) with a p-GaN capping layer.

Figure 4 shows the R_{ON} transient behaviors for both devices, where the measurements were made by simultaneously changing V_{GS} and V_{DS} from -3 and 10 V (OFF-state) to 3 and 0.5 V (ON-state), respectively. Agilent B1500A semiconductor parameter analyzer with a WGFMU module is used in our experiments. Figure 4 shows that R_{ON} of the device with a p-GaN capping layer is much smaller than that of the device without a p-GaN capping layer, and exhibits a saturated value after much shorter time from the bias-changing event. This result is consistent with that in Fig. 3, and confirms that a p-GaN capping layer can act as an effective passivation layer in p-GaN gate AlGaN/GaN HFETs.

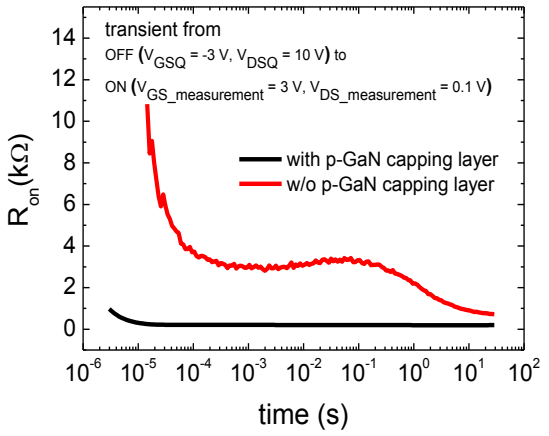

Fig. 4 R_{ON} transient behaviors for devices with and without a p-GaN capping layer.

Figure 5(a) and (b) show the time constant spectra extracted from R_{on} transient behaviors using the stretched exponential model at different temperatures, where Fig. 5(a) and (b) represent the extracted time constant spectra for devices without and with a p-GaN capping layer, respectively. In Fig. 5(a), a variety of time constants are observed, and they exhibit clear temperature dependence. Figure 5(c) shows the Arrhenius plot for the traps with time constants TP1 and TP2 in Fig. 5(a), which shows that the traps with times TP1 and TP2 are located around 0.27 and 0.28 eV below the conduction band, respectively. In Fig. 5(b), the results show that the time constants observed in Fig. 5(a) are disappeared, which represents that the traps in Fig. 5(c) are successfully removed by incorporating the p-GaN capping layer in p-GaN gate AlGaN/GaN HFETs.

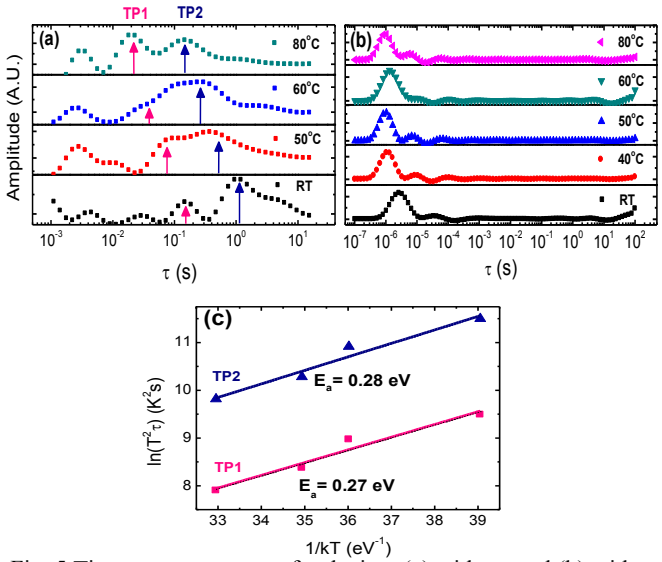

Fig. 5 Time constant spectra for devices (a) without and (b) with a p-GaN capping layer extracted from R_{on} transient behaviors at different temperatures. (c) Arrhenius plot for the traps with time constant TP1 and TP2 in Fig. 5(a).

4. Conclusions

In this work, we have investigated the effects of p-GaN capping layer in normally-off p-GaN gate AlGaN/GaN HFETs. No significant difference was observed in the DC characteristics between the devices with and without a p-GaN capping layer, but a notable improvement was observed in the current collapse behaviors in devices with a p-GaN capping layer. Our experimental results show that a p-GaN capping layer can effectively reduce the surface trapping effects in p-GaN gate AlGaN/GaN HFETs.

Acknowledgements

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