

Evaluation of Fully Implanted Lightly Doped Drain (LDD) GaN-MISFET for Low Voltage and High Frequency Applications

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I. Introduction

AlGaIn/GaN high electron mobility transistors (HEMTs) are widely investigated for power electronic applications, because of the attractive material properties of GaN such as large critical electric field, high electron mobility and good thermal conductivity¹. 2D electron gas (2DEG) drift regions^{2,3} are commonly used for GaN devices, which is beneficial for achieving low R_{on} and high voltage operation simultaneously. Typical examples are hetero-junction FET (HFET) and MIS-HEMT^{4,5}. On the other hand, complex epitaxial layer structures, limited gate isolation (HFET) and normally-on behavior (MIS-HEMT) are the disadvantages of the conventional AlGaIn/GaN HEMTs (Table. 1).

In this paper, we propose a novel concept of fully-implanted LDD GaN MISFET, which do not utilize the 2DEG regions. The proposed device is cost-effective, and can achieve superior performance for low voltage (<100V) and high frequency (~1MHz) applications.

II. Device Concept

A schematic cross-section of the proposed LDD MISFET is shown in Fig.1. Instead of the 2DEG, an implanted LDD drift region is used. The negative impact of the higher LDD resistance than 2DEG and lower channel mobility is not serious for low voltage devices, because the channel and drift regions are short. On the other hand, the GaN MISFET benefits from simpler substrate structure, lower contact resistance (R_{CT}), stronger gate isolation, and normally-off operations. Much higher performance than Si vertical power devices at reasonably low cost is expected, thanks to the nature of GaN and low parasitic capacitance of the lateral device architecture.

III. Experimental

GaN MISFETs were fabricated using un-doped GaN on Si substrates. N and P regions were formed by implanting Si and Mg ions. Fig. 2 shows the I_d - V_g characteristics of an LDD MISFET exhibiting normally-off operation. The roll-off properties of our LDD MISFET (Fig.3) shows that, by adjusting the

Pwell dose, threshold Voltage (V_{th}) around 1V is achieved down to channel length $L_{CH} = 0.25\mu m$ (Fig. 3). By using such short L_{CH} , both the channel resistance (R_{CH}) and gate charge Q_g can be reduced. The sheet resistance of N^+ -GaN and LDD can be controlled by the Si dose (Fig. 4). It can be even made lower than the 2DEG resistance, to reduce the contact resistance R_{CT} at N^+ -GaN. The low R_{CH} and R_{CT} can compensate the relatively high LDD sheet resistance. To minimize the LDD resistance, it is important to reduce its length, while keeping the electric field low. Therefore, gate and source field plate structures were examined. It was confirmed that they are effective for LDD MISFETs, as well as HEMT devices (Fig. 5). The excellent thermal stability of V_{th} and R_{on} was also obtained (Fig. 6). Compared with Si vertical MOSFETs⁷, the LDD MISFET designed for $V_{bd}=200V$ indicates much lower $R_{on}Q_g$ (Fig. 7).

The high frequency performance of the LDD MISFET devices was evaluated by forming a buck converter circuit (Fig. 8). Thanks to the gate isolation and the normally-off characteristics, the same circuit configuration could be used for both GaN and Si. The $R_{on}Q_g$ of the reference Si MOSFET was twice that of the LDD MISFET. The switching waveforms at 300 kHz clearly show that the LDD MISFETs realize much faster switching than the Si MOSFETs (Fig. 9). Circuit simulation predicts that LDD MISFETs optimized for minimizing parasitic resistance will achieve much higher efficiency than Si devices in the MHz regime (Fig.10). Over 90% efficiency at 2MHz can be expected.

IV. Conclusion

A new GaN LDD power MISFET concept for low voltage applications is proposed and its feasibility was demonstrated. Normally-off devices with much higher performance than Si devices can be realized.

References

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Table. 1 Characteristics of GaN transistor. Number of GaN layer determines the cost of substrate. Mobility determines the gate-drain resistance. Rated voltage of gate-source (V_{GS}) is generally $\sim 20V$ on Si-MOS power devices.

	HEMT		This work LDD-MISFET
	HFET	MIS-HEMT	
Structure			
GaN Layer	3~	2~	Mono layer
Mobility	$\odot$	$\odot$	$\blacktriangle$
Rated V_{GS}	$\sim 5V$	$\sim 20V$	$\sim 20V$
Normally-off	$\odot$	$\blacktriangle$	$\odot$

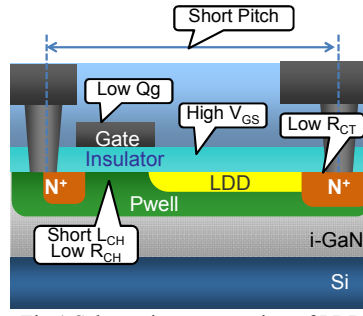


Fig.1 Schematic cross-section of LDD MISFET. High concentration impurity realize the short channel length (L_{CH}) and low contact resistance (R_{CT}).

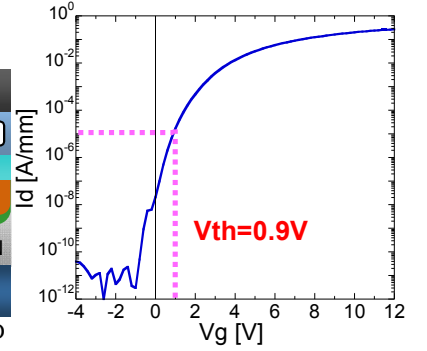


Fig.2 I_d - V_g Curve of LDD MISFET. V_{th} : 0.9V indicates Normally-off operation.

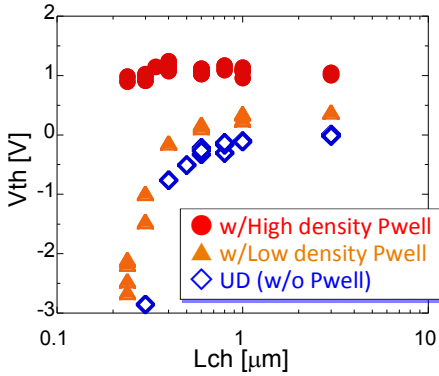


Fig.3 Roll-off characteristics of V_{th} depend on Pwell impurity density. High concentration Pwell realized stable normally-off operation irrespective of L_{ch} from 1 μm to 0.24 μm , which leads to low R_{CH} & low Q_g .

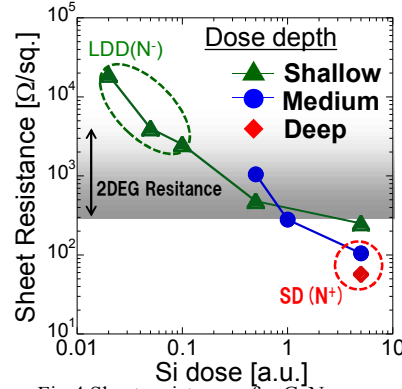


Fig.4 Sheet resistance of n-GaN as a function of Si dose. N^+ -GaN with high Si dose and deep Si dose achieved low resistance below the 2DEG resistance.

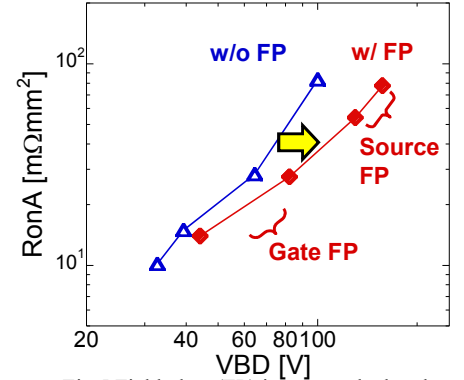


Fig.5 Field plate (FP) improves the breakdown voltage (V_{BD}) without increase the R_{onA} . Both Gate FP and Source FP are effective.

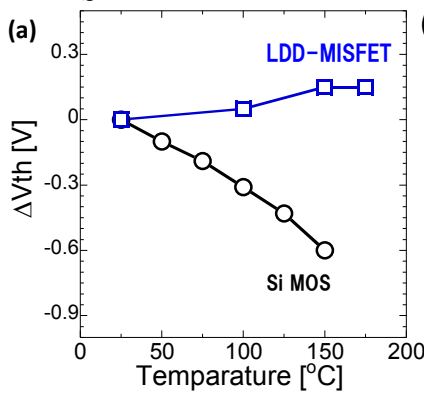


Fig.6 Thermal stability of (a) V_{th} and (b) R_{on} , between LDD MISFET and Si-MOS. V_{th} and R_{on} of LDD MISFET are stable up to high temperature range ($\sim 175^\circ C$).

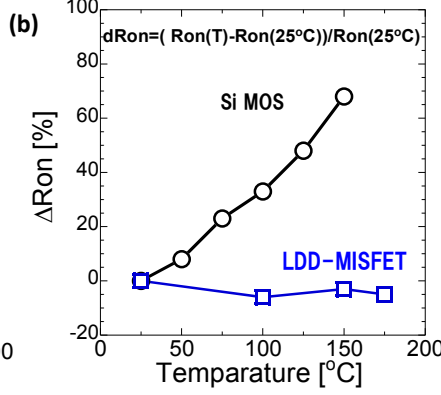


Fig.7 $R_{on}Q_g$ of Si-MOS and LDD MISFET. LDD MISFET has the extremely lower $R_{on}Q_g$ in low voltage region. (V_{GS} : 10V)

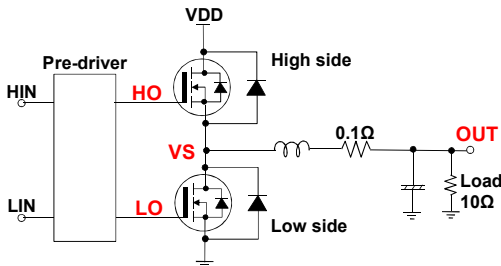


Fig.8 Back converter circuit for evaluation of high frequency applications. Only the both HO and LO transistor are changed to LDD MISFET or conventional Si-MOS. In this test, conventional driver was used with the same conditions ($V_{DD} = 10V$, $V_{CC} = 10V$, Load=10 Ω .)



Fig.9 Comparison of switching operation at 300 kHz between Si-MOS and LDD MISFET. For example, LO switching has sharp leading edge for LDD MISFET. Even though LDD MISFET has larger R_{on} than ideal value (due to unwanted PKG resistance), low Q_g realized low loss operation.

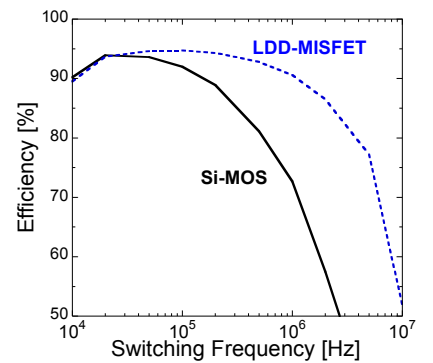


Fig.10 Estimation of device efficiency for high frequency region. In this Sim., LDD MISFET assumed the R_{on} has no PKG resistance. Ideal LDD MISFET keeps high efficiency over MHz frequency.