

Analysis on trade-off between drain resistance and drain-source capacitance of source field plate GaN HEMT

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Abstract

In this paper, a trade-off relationship between drain resistance (Rd) and drain-source capacitance (Cds) of source field plate (SFP) GaN HEMT is investigated quantitatively to optimize the device structure. It was found that there exists a knee point, beyond which Rd remains constant while Cds continues to rise. Efficiencies are calculated for structures which have the various SFP lengths from the T-CAD results. It was found that power added efficiency (PAE) exhibits highest value at that knee point. This is in good agreement with measurement result.

1. Introduction

GaN features higher breakdown voltage, higher saturation velocity and better thermal conductivity compared with existing semiconductor materials of GaAs and Si. Therefore, GaN is becoming a major material for high power and high frequency microwave amplifiers. These days, GaN HEMTs (High Electron Mobility Transistor) with more than 100W output power and more than 60% power added efficiency (PAE) are available [1]. However, details of electronic trapping effects are still unknown. It sometimes causes degradation of PAE and is one of serious problems. It is believed that strong electric field concentrated at the drain side edge of the gate electrode is the source of such electronic trapping effects. Therefore, so-called source field plate (SFP) structure is often employed to reduce electric field at the gate edge. By expanding the SFP, concentration of electric field can be relaxed and drain resistance in RF operation (Rd) can be reduced. However, it increases drain-source capacitance (Cds) [2][3]. Therefore, trade-off between Rd and Cds should be investigated quantitatively to optimize the device structure.

In this paper, a trade-off relationship between Rd and Cds are analyzed. It was found that there exists a knee point, beyond which Rd remains constant while Cds continues to rise. Also efficiencies are calculated for structures which have the various SFP lengths from the T-CAD results. It was found that PAE exhibits highest value at that knee point. This is in good agreement with measurement result.

2. Method of simulation

The simulated structure for SFP GaN HEMT is shown in Fig.1. The length from gate center to the edge of the SFP is

defined as SFP length (Lsf). Small signal equivalent circuit parameters for various SFP length structures are extracted from S parameters which are calculated by T-CAD for the equivalent circuit shown in Fig.2 [4]. By using small signal equivalent circuit parameters and measured Rd, PAE is calculated according to the improved Raab's model [5]. Measured Rd is obtained from measured pulse current.

3. Simulation result of drain resistance and drain-source capacitance

Measured Rd and calculated Cds versus Lsf is shown in Fig.3. As can be seen in Fig.3, Rd decreases and Cds increases as enlarging Lsf. Moreover, there exists a knee point (Lsf=1 μ m), beyond which Rd remains constant while Cds continues to rise. This means Lsf=1 μ m structure is the best compromise to keep both Rd and Cds. Measured Rd and electric field at the edge of gate (Egate) versus Lsf is shown in Fig.4. Egate is the electric field at 0.5nm underneath AlGaIn surface. As can be seen in Fig.4, the Lsf dependence of Egate is same as Rd. This means reduced Egate suppresses charge and de-charging rate of electronic trap to reduce Rd. Egate remains constant beyond knee point. This reason is explained in Fig.5. Electric fields of short Lsf and long Lsf are shown in Fig.5 schematically. When Lsf is shorter than the knee point, electric field that peaks at gate edge overlaps with electric field that peaks at the SFP edge as shown in Fig.5(a). Therefore the electric field at gate edge increases below a knee point. Meanwhile, when Lsf is longer than a knee point, two electric fields, one that peaks at gate edge and the other that peaks at SFP edge, become independent for each other as shown in Fig.5(b). Therefore electric field at gate edge remains constant beyond knee point.

4. Simulation result of power added efficiency

To make sure that the knee point Lsf which has the best compromise for Rd and Cds, indeed exhibits highest PAE, PAE of the transistor is calculated for various Lsf. PAE versus Lsf is shown in Fig.6. When Lsf is below 1 μ m, PAE increases as enlarging Lsf, because Rd decreases. When Lsf is beyond 1 μ m, PAE decreases as enlarging Lsf, because Cds increases while Rd remains constant. As shown in Fig.6, the structure which has a knee point shows highest PAE, as was expected. Calculated PAE is in good agreement with measured PAE.

5. Conclusion

A trade-off relationship between R_d and C_{ds} were analyzed. It was found that there exists a knee point, beyond which R_d remains constant while C_{ds} continues to rise. Efficiencies were calculated for structures which have various SFP lengths from the T-CAD results. It was found that PAE exhibits highest value at that knee point. This result is in good agreement with measured PAE.

References

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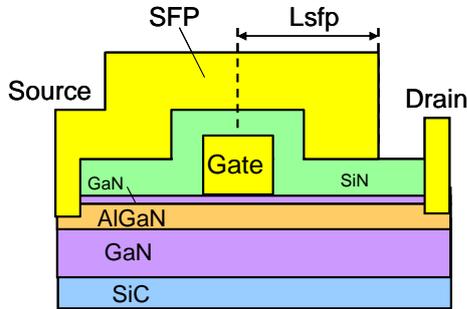


Fig.1 The simulation structure for SFP GaN HEMT

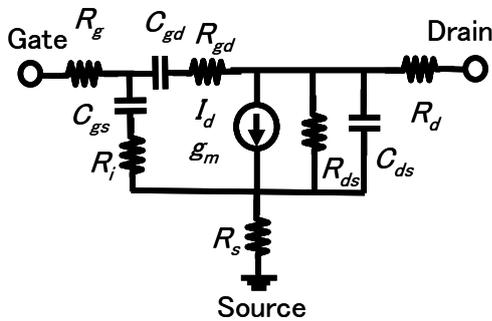


Fig.2 An equivalent circuit of GaN HEMT

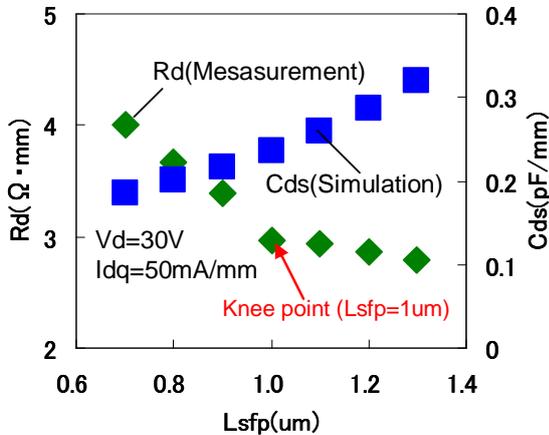


Fig.3 R_d (measurement) and C_{ds} (Simulation) vs SFP length (L_{sfp})

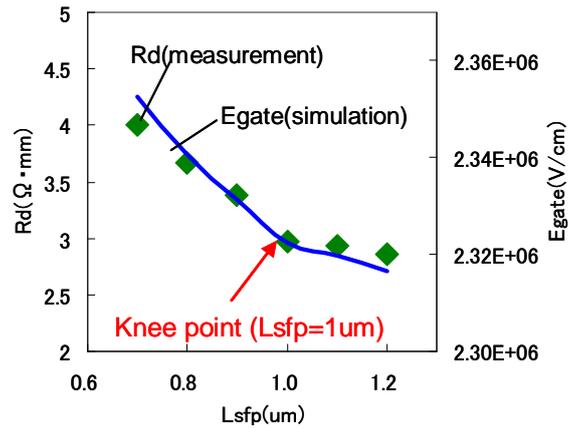
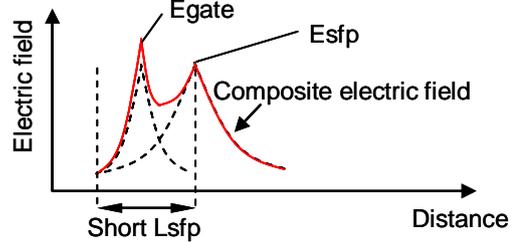
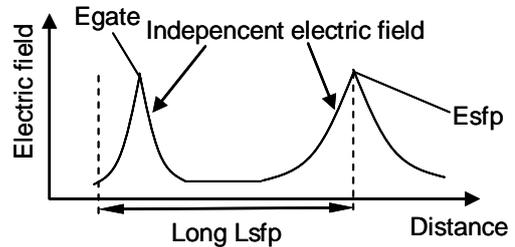


Fig.4 R_d (measurement) and E_{gate} (simulation) versus SFP length (L_{sfp}). E_{gate} is electric field at gate edge.



(a)



(b)

Fig.5 Schematic electric field distribution (a) short SFP length (b) long SFP length. E_{gate} and E_{sfp} are the peaks of electric field at the gate edge and source field plate, respectively.

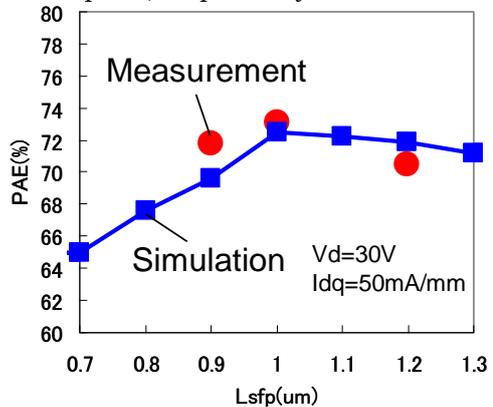


Fig.6 PAE vs SFP length (L_{sfp})