Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp968-969

Temperature-dependent Characteristics of AlGaN-GaN-on-Si Heterojunction Field Effect Transistors (HFETs) under reverse gate bias stress

Dongmin Keum[1], Shinhyuk Choi[1], Youngjin Kang[1], Jae-Gil Lee[1], Ho-Young Cha[1] and Hyungtak Kim[1]

[1] School of Electrical Engineering
Hongik University, Seoul 121-791, Korea, Republic of.
Phone: +82-2-320-3013 E-mail: rmaehdalf@hanmail.net

Abstract

We have performed the reverse gate bias stress test on AlGaN/GaN-on-Si HFETs and investigated the temperature dependence of the degradation characteristics. The shift of threshold voltage and the reduction of on-current were observed from the stressed device. As the temperature during the stress test increased, the changes of the threshold voltage and the on-current were decreased. The degradation was fully recovered in the ambient storage. Our experimental results suggest that electron trapping effect into shallow traps is the main cause of the observed degradation.

1. Introduction

GaN-based transistors have been intensively developed and are being commercialized in the high frequency applications over X-band. Before commercialization, tremendous efforts have been made to figure out the degradation mechanism of these devices and improve the reliability. [1,2] GaN-on-Si technology is aiming at high voltage application and the reliability at high temperature is a critical concern.

In this work, the reverse gate bias stress tests have been performed on AlGaN/GaN-on-Si HFETs with varying temperatures. The stressed devices showed the temperature dependence of the threshold voltage(V_{th}) shift and the on-current reduction without the gate current increase.

2. Device Fabrication

The tested devices were fabricated on GaN-on-Si epi structures of which the schematic cross-sectional view is shown in Fig. 1. After SiN prepassivation and mesa isolation, S/D ohmic contacts were formed by an e-beam evaporated Si/Ti/Al/Mo/Au (5/20/60/35/50 nm) metal stack onto ohmic recess and alloyed by RTA. A Ni/Pt/Au (20/20/100 nm) metal stack was evaporated for the gate electrode formation. A post RTA annealing was carried at 400 ℃ for 5 min in N_2 ambient to decrease the gate leakage current [3,4] The gate-to-drain distance, gate length, and gate-to-source distance were 20 um, 2 um, and 3 um, respectively. There are no gate field plates.

3. Stress Experiments

AlGaN/GaN HFETs on Si substrate were submitted to reverse gate step bias stress test at a room temperature (RT). The applied bias was stepped from -11 V to -50 V by -1 V and maintained for 1 minute at each step. As shown in Fig. 2(a), the gate leakage current was increased gradually contrary to the previous reports in which the sudden increase of gate leakage was observed. [5-7] Fig. 2(b) also shows that the stressed device demonstrated the positive shift of the threshold voltage and the reduction of on-current with the stress test being progressed.

We performed the stress tests at the elevated baseline temperatures of 60, 80, 100, and, 120 ℃, respectively to investigate the temperature dependence of the degradation. Similarly to the stress test at a RT, the gate leakage currents were gradually increased. (Fig. 2(a)) However, transfer IV (Fig. 3) and output IV characteristics (Fig. 4) shows the shift of V_{th} and the reduction of on-current were decreased as the temperature increased. No significant changes of V_{th} and on-current were observed at the temperatures over 100 C. The degradation of gate current was negligible at all tested temperatures. The stressed devices were recovered in the ambient storage at a RT. The changes of the device characteristics are summarized in Fig. 5 (a).

4. Discussions

It has been widely reported that reverse gate bias stress results in the sudden increase of the gate leakage current due to the defect generation by an inverse piezoelectric effect and this degradation is permanent.[5-7] However, any symptom of inverse piezoelectric effect was noticed in our experiment. Instead, the shift of V_{th} was observed and the reduction of on-current was accompanied. Hot electron effect, which can induce the channel depletion and reduce the on-current [8], is not a concern in our stress condition where the drain and the source are grounded together. In our experiments, electrons are trapped into the layers underneath the gate and these negative charges give rise to the positive shift of V_{th} and thereby reduce the on-current. [9] The nature of the traps is likely to be very shallow because the trapped charges are reduced, i.e., the detrapping process is enhanced as the temperature increases from a RT to 100 ℃. The shift of V_{th} was fully recoverable and it suggests that trapped electrons were mostly released from the shallow traps at a RT. In Fig. 5 (b), the activation energy of the degradation has been extracted from the temperature-dependent parameters of ΔV_{th} and ΔI_{ds}. The extracted activation energies were 0.16 eV and 0.18 eV from ΔV_{th} and ΔI_{ds}, respectively, and the small values indicate the shallow nature of the traps. [10] The similar values of the

activation energy extracted from the two different parameters suggest that the reduction of I_{ds} can be strongly linked to the shift of V_{th}. The origin of traps is likely to be related to the gate opening etch process through the SiN pre-passivation layer. Further investigation is necessary to identify the origin of traps.

4. Conclusions

We performed the reverse gate bias stress tests on AlGaN/GaN-on-Si HFETs to investigate the degradation characteristics varying temperatures. The positive shift of V_{th} and the decrease of on-current were observed and the changes of the device parameters were reduced as temperatures increased. Our results suggest that observed degradation was dominated by the electron trapping into the shallow traps under the gate region which can be recovered by the detrapping process.

Acknowledgements

This research was supported by the Basic Science Research Program (2013022217) through the NRF funded by the Ministry of Education, Science and Technology of Korea.

References

[1] J.A. del Alamo *et al*, Microelectron. Reliab. **49** (2009) 1200.

[2] G. Meneghesso *et al*, IEEE Trans. Device Mater. Rel. **8** (2008) 332.

[3] N. Miura *et al*, Solid-State Electron. **48** (2004) 689.

[4] J. Lee *et al*, Solid-State Electron. **48** (2004) 1855.

[5] J. Joh *et al*, *IEEE IEDM tech. digest.* (2006) 1.

[6] D. Marcon *et al*, *IEEE IEDM tech. digest.* (2010) 20.3.1.

[7] E. A. Douglas *et al*, *IEEE IIRW workshop.* (2010) 125.

[8] H. Kim *et al*, IEEE Electron. Dev. Lett, **24** (2003) 421.

[9] M. Caesar *et al*, *IEEE IRPS proc.* (2012) C.D.6.1.

[10] H. Kim *et al*, Appl. Phys. Lett. **86**, (2005) 143505.

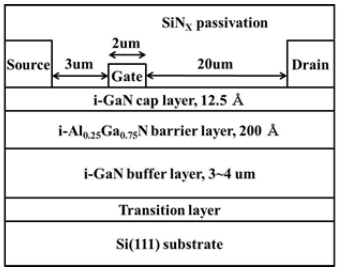

Fig. 1 Fig. 1 Device Structure of AlGaN/GaN-on-Si HFET.

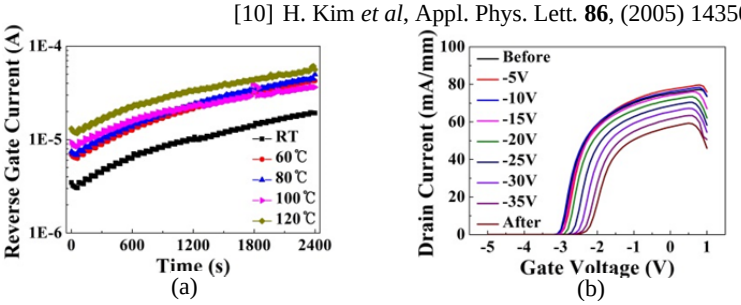

Fig. 2 (a) Gate leakage current during the reverse gate step bias stress tests with V_{DS}=0 V (b) Transfer I-V characteristics meas ured at V_D=1 V before and after stress test.

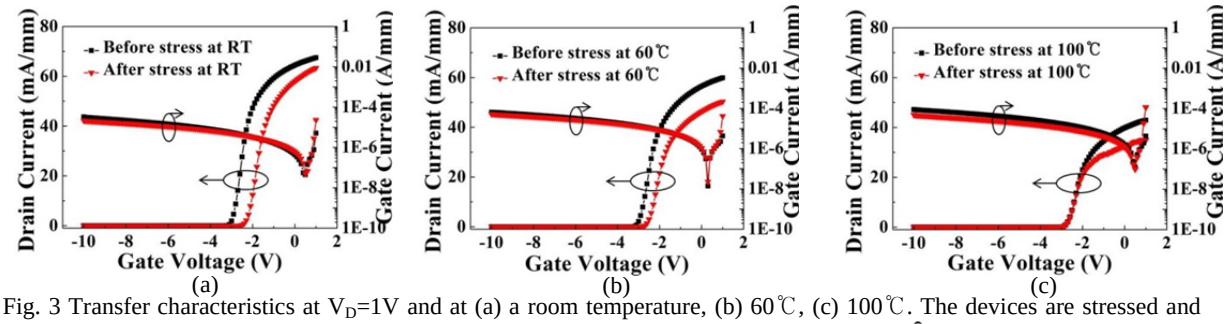

Fig. 3 Transfer characteristics at V_D=1V and at (a) a room temperature, (b) 60℃, (c) 100℃. The devices are stressed and measured at the specified temperatures.

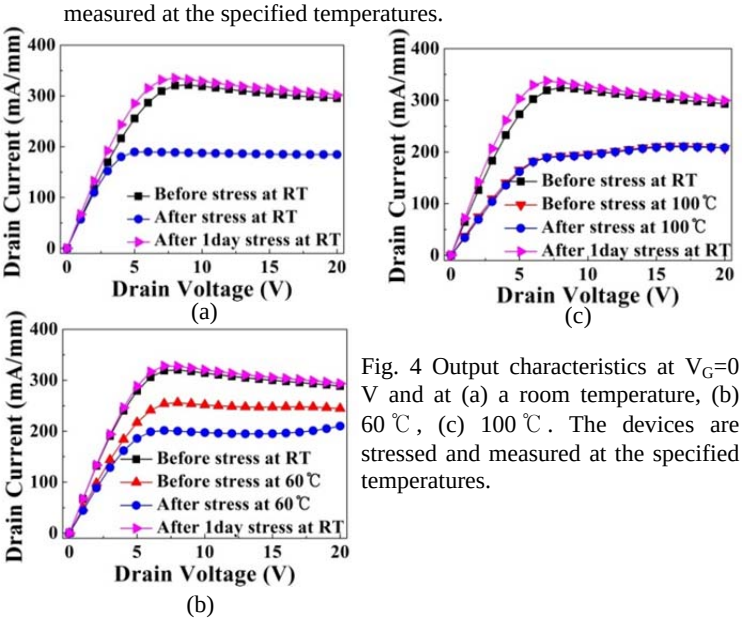

Fig. 4 Output characteristics at V_G=0 V and at (a) a room temperature, (b) 60℃, (c) 100℃. The devices are stressed and measured at the specified temperatures.

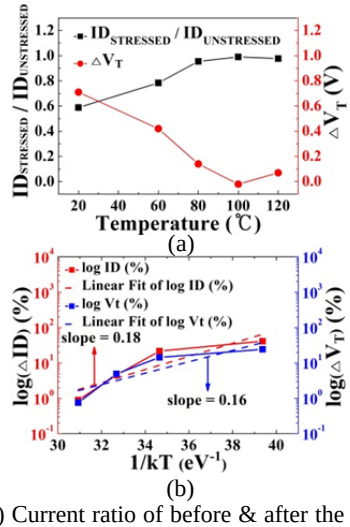

Fig. 5 (a) Current ratio of before & after the stress and ΔV_T at the different temperatures. (b) Activation energy extracted from the temperature dependence of ΔV_T and ΔI_D.