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$P_2S_5/(NH_4)_2S_x$-Based Sulfur Mono-Layer Doping Technique to form Sub-10 nm Ultra-Shallow Junctions for Advanced III-V Logic Devices

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Abstract

We report the first ultra-shallow junctions on InGaAs using sulfur mono-layer doping (SMLD) to achieve sub-10 nm junctions with sheet resistances < 150 Ω/□. An 8 nm junction with low sheet resistance of ~130 Ω/□ was achieved by SMLD using $P_2S_5/(NH_4)_2S_x$ solution. Addition of P_2S_5 to $(NH_4)_2S_x$ resulted in a 50% reduction in junction depth at a low thermal budget of 550 °C. InGaAs nMOSFETs with S/D formed using SMLD were demonstrated. The effects of dopant activation conditions on the performance of devices formed using a gate-first scheme is evaluated.

I. Introduction

III-V materials such as InGaAs and InAs are promising candidates to replace silicon as the channel for nMOSFETs in future technology nodes due to their high electron mobilities. At such extremely scaled dimensions, ultra-thin body (UTB) or FinFET structures (Fig. 1) would be required to suppress short channel effects (SCE). These devices require ultra-shallow junctions (USJ) to form the source/drain (S/D) or S/D extensions. A uniform, conformal, and damage free doping technique would be important to ensure good device performance. SMLD would be a promising technology option to achieve these goals [1-3].

In this paper, we demonstrate for the first time, USJ (sub-10 nm) with sheet resistance R_{sh} < 150 Ω/□ formed by SMLD that satisfy the ITRS requirements for S/D junctions at sub-22 nm nodes [4]. In this work, a novel technique for achieving a more abrupt junction, by adding phosphorus pentasulfide (P_2S_5) to the conventional $(NH_4)_2S_x$-based SMLD, was demonstrated. The first n-channel InGaAs MOSFET that employ SMLD technique for S/D junction formation was also demonstrated.

II. Mono-layer Doping of InGaAs using P_2S_5 and $(NH_4)_2S_x$

A. Motivation for using P_2S_5

In the past, P_2S_5 has been added to $(NH_4)_2S_x$ and NH_4OH for the passivation of GaAs surfaces [5-7]. The addition of P_2S_5 improves the surface coverage of sulfur (S) atoms and increases the robustness of the layer as it degrades more slowly when exposed to air [8]. It has also been reported that addition of P_2S_5 to $(NH_4)_2S_x$ reduces the surface roughness of the sample after treatment [9]. This is important for achieving good contacts. SMLD was carried out using three solutions: $(NH_4)_2S_x$ (20% in H_2O), $P_2S_5/(NH_4)_2S_x$, and P_2S_5/NH_4OH. The concentration of P_2S_5 in $(NH_4)_2S_x$ and NH_4OH solutions was 1.6 mg/ml.

B. Sample Preparation

Key steps illustrating the SMLD technique on InGaAs are shown in Fig. 2. The starting substrate consists of a 500 nm p-type (2×10^{16} cm^{-3}) $In_{0.53}Ga_{0.47}As$ epitaxially grown on InP substrate. A pre-clean [HCl:H_2O (1:3)] removed native oxide from the sample surface prior to SMLD. The samples were then treated with S-containing solutions at room temperature for 30 minutes. The samples were loaded into an e-beam evaporator tool without rinsing. A silicon dioxide (SiO_2) capping layer (15 nm) was then deposited, which would act as a capping layer to prevent out-diffusion of S during dopant activation. The samples were annealed using a rapid thermal process (RTP) for driving in the S atoms and dopant activation.

C. Material Characterization

After removing the SiO_2 capping layer from the samples, four-point probe measurements were performed to extract R_{sh}. Fig. 3(a) shows the dependence of R_{sh} on annealing temperature. For a 300 s anneal, R_{sh} decreases from ~500 to ~20 Ω/□ as the temperature is increased from 550 to 700 °C. At 600 °C, R_{sh} decreases from values higher than 200 to ~80 Ω/□ as the annealing time is increased from 60 to 300 s as shown in Fig. 3(b). The higher R_{sh} for samples with P_2S_5 annealed at 550 °C for 300 s and 600 °C for 60 s could be caused by lower activation efficiency of S or a reduction in electron mobility, due to the introduction of phosphorus (P) into InGaAs.

Fig. 4(a) compares the S profiles obtained using Secondary Ion Mass Spectroscopy (SIMS) after treatment in $P_2S_5/(NH_4)_2S_x$ and $(NH_4)_2S_x$ solutions, followed by a 550 °C anneal for 300 s. The addition of P_2S_5 results in a steeper S profile with a slope of 1.3 nm/decade (dec.) and junction depth X_j of 5 nm (X_j is defined at S concentration of 5×10^{18} cm^{-3} [3]). The steeper profile could be due to the effect of the addition of P atoms on the diffusion of S atoms into InGaAs. Fig. 4(b) shows the S profiles in $P_2S_5/(NH_4)_2S_x$ after 600 °C anneal for 60 and 180 s, which show the formation of 6 and 8 nm junctions, respectively.

Fig. 5 benchmarks the R_{sh} vs X_j values achieved. Improvement from the previous results reported of SMLD on InGaAs has been achieved, in terms of lower X_j and a significant reduction in R_{sh}.

III. First n-channel InGaAs MOSFET with S/D formed using SMLD

A. Device Fabrication

The process flow and schematics for the fabrication of the MOSFETs are shown in Fig. 6. $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ on InP substrate was used as the starting wafer. Pre-gate clean using HCl, NH_4OH and $(NH_4)_2S_x$ solutions was carried out to remove any native oxide and impurities on the InGaAs surface. This was followed by gate stack deposition and post deposition anneal at 300 °C for 60 s. The gate stack consists of Al_2O_3 dielectric (5.5 nm) and TaN metal gate. After gate patterning, samples were treated with the $P_2S_5/(NH_4)_2S_x$ solution for 30 minutes and capped with SiO_2 (15 nm). Samples were then annealed under different conditions for the S/D formation. Devices were isolated with a mesa etch and PdGe contacts were formed to complete the fabrication.

B. Electrical Characteristics

I_{DS}-V_{GS}, $G_{M,int}$-V_{GS}, and I_{DS}-V_{DS} characteristics of a MOSFET with L_G of 1 μm are shown in Figs. 7-9. The S/D of this device was formed at 600 °C for 180 s. Intrinsic peak transconductance $G_{M,int}$ of ~140 μS/μm at V_{DS} = 1.1 V was obtained, as shown in Fig. 9. The device has a large parasitic S/D series resistance (R_{SD}) due to the large distance (5 μm) between the PdGe contacts and the metal gate, and the current has to flow through 5 μm of the ultra-shallow n^{++} layer. In a state-of-the-art device, this distance would be reduced by several hundred times.

The effect of dopant activation conditions on the performance of the device was evaluated. Fig. 10 shows that there is a significant reduction in both the on-state current I_{ON} (at V_{GS}-V_T of 1 V) and peak $G_{M,int}$ as we increase the annealing temperature and time. This can be attributed to the degradation of the interface between the gate dielectric and the channel due to higher thermal budget. The gate stack deterioration observed can be avoided by using a gate-last scheme during device fabrication.

A comparison of SMLD, using $P_2S_5/(NH_4)_2S_x$ to that using conventional $(NH_4)_2S_x$ that has been previously reported is shown in Table I. In addition to reductions in both X_j and R_{sh}, the junctions in this work have been formed at a lower thermal budget of 550 and 600 °C using $P_2S_5/(NH_4)_2S_x$.

IV. Conclusion

We have demonstrated the first SMLD process on InGaAs that has achieved sub-10 nm junctions with R_{sh} < 150 Ω/□. Addition of P_2S_5 in $(NH_4)_2S_x$ helps in achieving steeper S profiles. The results achieved here indicate great promise for the use of SMLD technique in future logic device applications. The dopant activation conditions need to be optimized in order to achieve high-performance MOSFETs.

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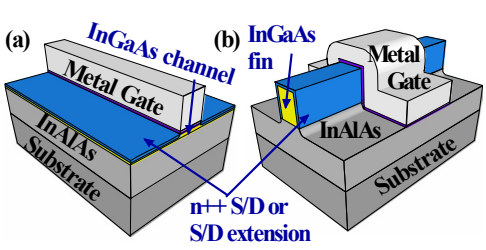

Fig. 1. Device structures that are candidates for future technology nodes such as (a) UTB-MOSFETs and (b) FinFETs require uniform, conformal, and damage-free doping technology.

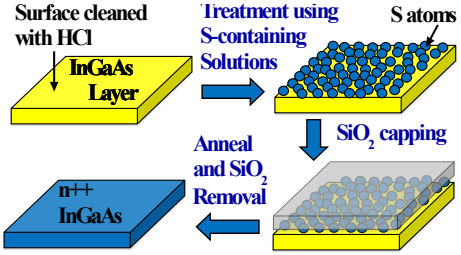

Fig. 2. The MLD process consists of a pre-clean with HCl, followed by treatment in a S-containing solution. The sample is then capped with SiO_2 and annealed to form the n^{++} region.

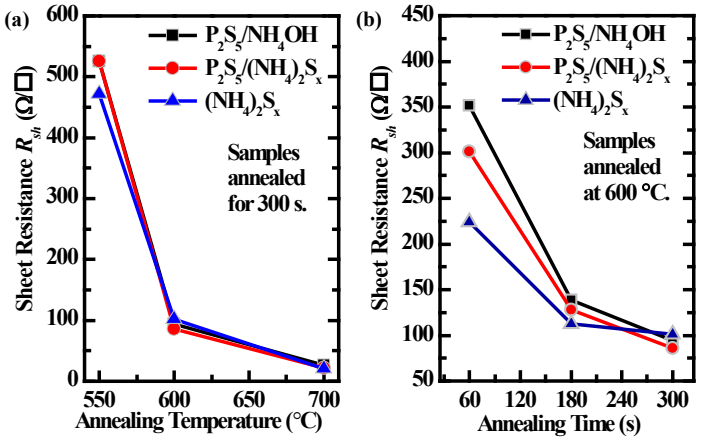

Fig. 3. R_{sh} of samples annealed at different (a) temperatures, and (b) times. R_{sh} < 150 Ω/square was obtained.

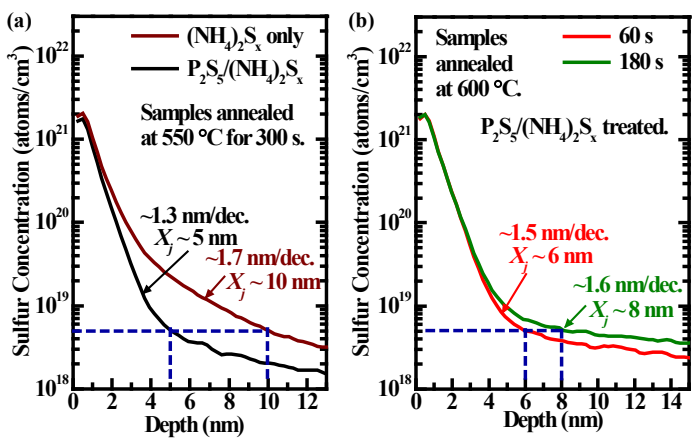

Fig. 4. SIMS profiles of junctions formed at different annealing (a) temperatures, and (b) times. Sub-10 nm junctions were achieved. X_j was defined at $5x10^{18}$ cm^{-3}.

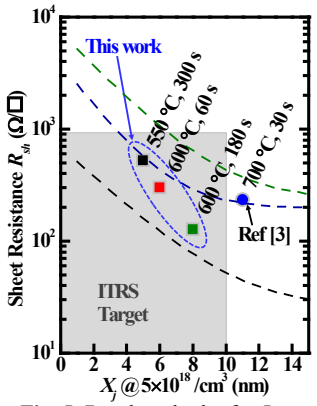

Fig. 5. Benchmark plot for R_{sh} vs X_j. An 8 nm junction with a R_{sh} of 130 Ω/□ was achieved. The gray region indicates the ITRS targets.

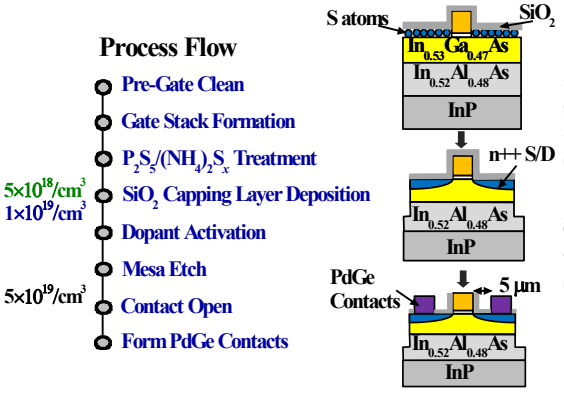

Fig. 6. Process flow, and schematics for the fabrication of InGaAs nMOSFETs using SMLD to form the S/D.

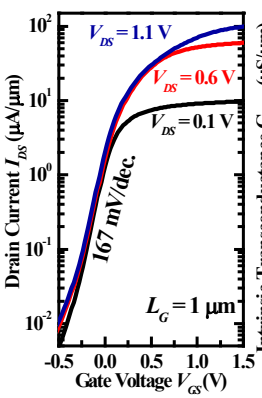

Fig. 7. I_{DS}-V_{GS}. The S/D was formed at 600 °C, 180 s. The device exhibits good transfer characteristics.

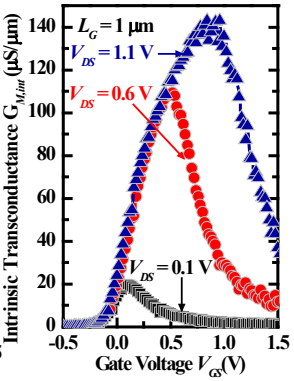

Fig. 8. Peak G_M of 140 µS/µm at V_{DS} of 1.1 V can be observed in the $G_{M,int}$-V_{GS} plot shown.

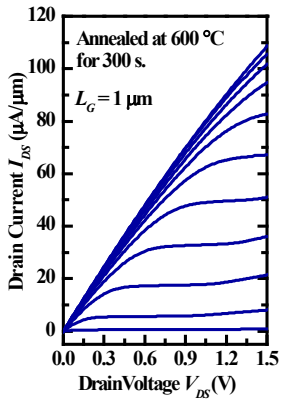

Fig. 9. I_{DS}-V_{DS} plot with gate overdrive (V_{GS}-V_T) varying from 0 to 2 V in steps of 0.2 V.

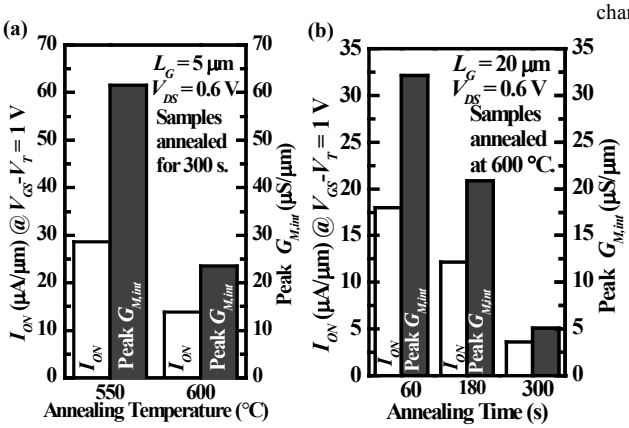

Fig. 10. I_{ON} at V_{GS}-V_T = 1 V and peak $G_{M,int}$ at V_{DS} of 0.6 V, for samples annealed at different (a) temperatures and (b) times. Reduction in both the I_{ON} and peak $G_{M,int}$ was observed at higher thermal budget. This can be attributed to the degradation of the gate stack.

Table I. Summary of the SMLD process using $P_2S_5/(NH_4)_2S_x$ highlighting improvements over previous results.

		Reference [3]				This Work		
Sulfur Solution		$(NH_4)_2S_x$				$P_2S_5/(NH_4)_2S_x$		
Pre-Clean		DHF (1:100)				HCl (1:3)		
Treatment Conditions	Temp. (° C)	35				25		
	Time (minutes)	5-10				30		
Capping Layer	Material	Al_2O_3		SiN/ Al_2O_3	SiN/ BeO	SiO_2		
	Temp. (° C)	30	100	30/250	30/250	25		
Annealing Conditions	Temp. (° C)	700				600		550
	Time (s)	30				180	60	300
R_{sh} (Ω/□)		278	382	297	232	127	301	525
X_j (nm) at $5x10^{18}$ cm^{-3}		~18	~16	~14	~11	~8	~6	~5