Abstract

We report the first ultra-shallow junctions on InGaAs using sulfur mono-layer doping (SMLD) to achieve sub-10 nm junctions with sheet resistances < 150 Ω/□. An 8 nm junction with low sheet resistance of ~130 Ω/□ was achieved by SMLD using P$_2$S$_5$/(NH$_4$)$_2$S$_x$ solution. Addition of P$_2$S$_5$ to (NH$_4$)$_2$S resulted in a 50% reduction in junction depth at a low thermal budget of 550 °C. InGaAs nMOSFETs with S/D formed using SMLD were demonstrated. The effects of dopant activation conditions on the performance of devices formed using a gate-first scheme is evaluated.

I. Introduction

III-V materials such as InGaAs and InAs are promising candidates to replace silicon as the channel for nMOSFETs in future technology nodes due to their high electron mobilities. At such extremely scaled dimensions, ultra-thin body (UTB) or FinFET structures (Fig. 1) would be required to suppress short channel effects (SCE). These devices require ultra-shallow junctions (USJ) to form the source/drain (S/D) or S/D extensions. A uniform, conformal, and damage free doping technique would be important to ensure good device performance. SMLD would be a promising technology option to achieve these goals [1-3].

In this paper, we demonstrate for the first time, USJ (sub-10 nm) with sheet resistance $R_{sh} < 150$ Ω/□ formed by SMLD that satisfy the ITRS requirements for S/D junctions at sub-22 nm nodes [4]. In this work, a novel technique for achieving a more abrupt junction, by adding phosphorus pentasulfide (P$_2$S$_5$) to the conventional (NH$_4$)$_2$S-based SMLD, was demonstrated. The first n-channel InGaAs MOSFET that employ SMLD technique for S/D junction formation was also demonstrated.

II. Mono-layer Doping of InGaAs using P$_2$S$_5$ and (NH$_4$)$_2$S

A. Motivation for using P$_2$S$_5$

In the past, P$_2$S$_5$ has been added to (NH$_4$)$_2$S and NH$_4$OH for the passivation of GaAs surfaces [5-7]. The addition of P$_2$S$_5$ improves the surface coverage of sulfur (S) atoms and increases the robustness of the layer as it degrades more slowly when exposed to air [8]. It has also been reported that addition of P$_2$S$_5$ to (NH$_4$)$_2$S reduces the surface roughness of the sample after treatment [9]. This is important for achieving good contacts. SMLD was carried out using three solutions: (NH$_4$)$_2$S$_x$ (20% in H$_2$O), P$_2$S$_5$/(NH$_4$)$_2$S$_x$ and P$_2$S$_5$/NH$_4$OH. The concentration of P$_2$S$_5$ in (NH$_4$)$_2$S and NH$_4$OH solutions was 1.6 mg/ml.

B. Sample Preparation

Key steps illustrating the SMLD technique on InGaAs are shown in Fig. 2. The starting substrate consists of a 500 nm p-type (2×10$^{16}$ cm$^{-3}$) In$_{0.53}$Ga$_{0.47}$As epitaxially grown on InP substrate. A pre-clean [HCl/H$_2$O (1:3)] removed native oxide from the sample surface prior to SMLD. The samples were then treated with S-containing solutions at room temperature for 30 minutes. The samples were loaded into an e-beam evaporator tool without rinsing. A silicon dioxide (SiO$_2$) capping layer (15 nm) was then deposited, which would act as a capping layer to prevent out-diffusion of S during dopant activation. The samples were annealed using a rapid thermal process ( RTP) for driving in the S atoms and dopant activation.

C. Material Characterization

After removing the SiO$_2$ capping layer from the samples, four-point probe measurements were performed to extract $R_a$. Fig. 3(a) shows the dependence of $R_a$ on annealing temperature. For a 300 s anneal, $R_a$ decreases from ~500 to ~20 Ω as the temperature is increased from 550 to 700 °C. At 600 °C, $R_a$ decreases from values higher than 200 to ~80 Ω as the annealing time is increased from 60 to 300 s as shown in Fig. 3(b). The higher $R_a$ for samples with P$_2$S$_5$ annealed at 550 °C for 300 s and 600 °C for 60 s could be caused by lower activation efficiency of S or a reduction in electron mobility, due to the introduction of phosphorus (P) into InGaAs.

Fig. 4(a) compares the S profiles obtained using Secondary Ion Mass Spectroscopy (SIMS) after treatment in P$_2$S$_5$/(NH$_4$)$_2$S$_x$ and (NH$_4$)$_2$S$_x$ solutions, followed by a 550 °C anneal for 300 s. The addition of P$_2$S$_5$ results in a steeper S profile with a slope of 1.3 nm/decade (dec.) and junction depth $X_J$ of 5 nm ($X_J$ is defined at S concentration of 5×10$^{16}$ cm$^{-3}$) [3]. The steeper profile could be due to the effect of the addition of P atoms on the diffusion of S atoms into InGaAs. Fig. 4(b) shows the S profiles in P$_2$S$_5$/(NH$_4$)$_2$S$_x$ after 600 °C anneal for 60 and 180 s, which show the formation of 6 and 8 nm junctions, respectively.

Fig. 5 benchmarks the $R_a$ vs $X_J$ values achieved. Improvement from the previous results reported of SMLD on InGaAs has been achieved, in terms of lower $X_J$ and a significant reduction in $R_a$.

III. First n-channel InGaAs MOSFET with S/D formed using SMLD

A. Device Fabrication

The process flow and schematics for the fabrication of the MOSFETs are shown in Fig. 6. In$_{0.53}$Ga$_{0.47}$As/Si/SiO$_2$/TiN/Al$_2$O$_3$/Si on InP substrate was used as the starting wafer. Pre-gate clean using HCl, NH$_4$OH and (NH$_4$)$_2$S$_x$ solutions was carried out to remove any native oxide and impurities on the InGaAs surface. This was followed by gate stack deposition and post deposition anneal at 300 °C for 60 s. The gate stack consists of Al$_2$O$_3$ dielectric (5.5 nm) and TaN metal gate. After gate patterning, samples were treated with the P$_2$S$_5$/(NH$_4$)$_2$S$_x$ solution for 30 minutes and capped with SiO$_2$ (15 nm). Samples were then annealed under different conditions for the S/D formation. Devices were isolated with a mesa etch and PdGe contacts were formed to complete the fabrication.

B. Electrical Characteristics

$I_{DS}$-$V_{DS}$, $G_{M,int}$-$V_{DS}$, and $I_{DS}$-$V_{GS}$ characteristics of a MOSFET with $L_{G}$ of 1 μm are shown in Figs. 7-9. The S/D of this device was formed at 600 °C for 180 s. Intrinsic peak transconductance $G_{M,int}$ of ~140 μS/μm at $V_{DS}$ = 1.1 V was obtained, as shown in Fig. 9. The device has a large parasitic S/D series resistance (R$_{sd}$) due to the large distance (5 μm) between the PdGe contacts and the metal gate, and the current has to flow through 5 μm of the ultra-shallow n$+$ layer. In a state-of-the-art device, this distance would be reduced by several hundred times.

The effect of dopant activation conditions on the performance of the device was evaluated. Fig. 10 shows that there is a significant reduction in both the on-state current $I_{ON}$ (at $V_{DS}$=$V_{GS}$ of 1 V) and peak $G_{M,int}$ as we increase the annealing temperature and time. This can be attributed to the degradation of the interface between the gate dielectric and the channel due to higher thermal budget. The gate stack deterioration observed can be avoided by using a gate-last scheme during device fabrication.

A comparison of SMLD, using P$_2$S$_5$/(NH$_4$)$_2$S$_x$ to that using conventional (NH$_4$)$_2$S, that has been previously reported is shown in Table 1. In addition to reductions in both $X_J$ and $R_a$, the junctions in this work have been formed at a lower thermal budget of 550 and 600 °C using P$_2$S$_5$/(NH$_4$)$_2$S$_x$.

IV. Conclusion

We have demonstrated the first SMLD process on InGaAs that has achieved sub-10 nm junctions with $R_a$ < 150 Ω/□. Addition of P$_2$S$_5$ in (NH$_4$)$_2$S$_x$ helps in achieving steeper S profiles. The results achieved here indicate great promise for the use of SMLD technique in future logic device applications. The dopant activation conditions need to be optimized in order to achieve high-performance MOSFETs.

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REFERENCES

Fig. 1. Device structures that are candidates for future technology nodes such as (a) UTB-MOSFETs and (b) FinFETs require uniform, conformal, and damage-free doping technology.

Fig. 2. The MLD process consists of a pre-clean with HCl, followed by treatment in a S-containing solution. The sample is then capped with SiO2 and annealed to form the n+ region.

Fig. 3. Rsh of samples annealed at different (a) temperatures, and (b) times. Rsh < 150 Ω/square was obtained.

Fig. 4. SIMS profiles of junctions formed at different annealing (a) temperatures, and (b) times. Sub-10 nm junctions were achieved. Xj was defined at 5×10^15 cm^-2.

Fig. 5. Benchmark plot for Rsh vs Xj. An 8 nm junction with a Rsh of 130 Ω/µm was achieved. The gray region indicates the ITRS targets.

Fig. 6. Process flow, and schematics for the fabrication of InGaAs nMOSFETs using SMLD to form the S/D.

Fig. 7. Igat-VGS. The S/D was formed at 600 °C, 180 s. The device exhibits good transfer characteristics.

Fig. 8. Peak Gm of 140 μS/µm at VDS of 1.1 V can be observed in the Gm, VDS plot shown.

Table 1. Summary of the SMLD process using P2S5/(NH4)2Sx highlighting improvements over previous results.

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<td>DHF (1:100)</td>
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Fig. 9. Igat-VDS plot with gate overdrive (VGS-VT) varying from 0 to 2 V in steps of 0.2 V.

Fig. 10. Igat at VDS = 1 V and peak Gm at VDS of 0.6 V, for samples annealed at different (a) temperatures and (b) times. Reduction in both the Igat and peak Gm was observed at higher thermal budget. This can be attributed to the degradation of the gate stack.

Fig. 11. Process Flow.