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High Performance Silicon Waveguide-Integrated PIN and Schottky Ge Photodiodes and their Link with Inverter-Type CMOS TIA Circuits

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1. Introduction

Silicon photonics has recently attracted much attention because it offers low cost, low power consumption, and high bandwidth optoelectronic solutions for applications ranging from telecommunications down to chip-to-chip interconnects [1]. By integrating germanium into silicon photonics circuits, very efficient photodetection has been demonstrated for the past several years [2], [3].

Although the development of high speed and high efficiency Ge photodiodes (Ge PDs) has been reported, higher performance with low dark current density has not been achieved by practical fabrication process. The Schottky Ge-PD has an advantage over the PIN Ge-PD, because the n-type doping process to the Ge top layer and the ohmic-contact process with a metal electrode can be omitted.

In this paper, we first compare Si waveguide-integrated PIN and Schottky Ge PDs, which showed very low dark current density with high efficiency. An optimized PIN Ge PD showed a high speed of 50 GHz. We also report on a PIN Ge PD connected to an inverter-type CMOS (complementary metal-oxide-semiconductor) TIA (trans-impedance amplifier) circuit, which has a smaller footprint and showed a larger gain than those of a conventional analog-type CMOS-TIA.

2. Experiment

Figure 1 (a) and (b) show a schematic diagram and SEM image of the Si-waveguide-integrated PIN and Schottky Ge PDs. The fabrication process started with 4-inch silicon-on-insulator (SOI) wafers with a SOI thickness of 220 nm. The Si waveguides (Si-WGs) were patterned by electron beam lithography and dry etching. Then, B ions were implanted, and the wafers were annealed to form the p^+-Si of the bottom electrode. The 1.0-μm-thickness of epitaxial germanium mesas was selectively grown on the Si-WGs by reduced-pressure chemical vapor deposition method. A SiGe cap layer was deposited on the Ge layer to passivate the Ge surface. For the PIN Ge PD, P ion implantation was performed,; for the Schottky Ge PD, no P ion implantation was performed. Then, the 1-μm-thick SiO_2 upper-clad layer was deposited, and contact-holes were formed by UV lithography and dry-etching process. Finally, metal electrodes of Ti/TiN/Al layers were deposited and patterned.

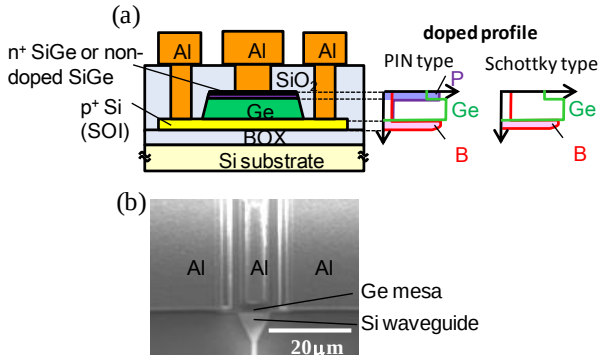

Fig. 1 (a) Schematic diagram and (b) SEM image of Si waveguide- integrated PIN and Schottky Ge PDs.

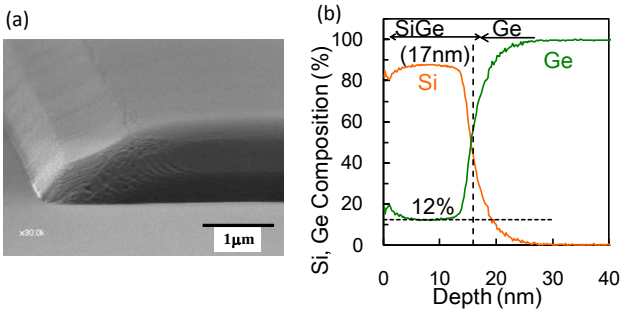

Fig. 2 (a) SEM image of selectively grown Ge with SiGe capping layers. (b) SIMS profile of Si and Ge in SiGe/Ge layers grown in optimized conditions [4].

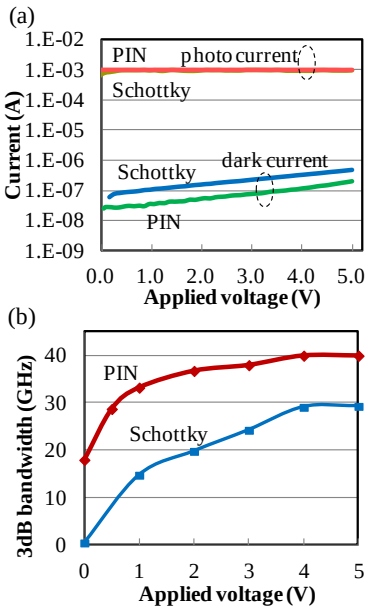

Fig. 3 (a) Photoresponsivity and (b) 3dB bandwidth of fabricated PIN and Schottky Ge PDs.

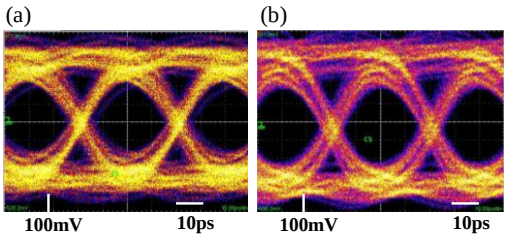

Fig. 4 Measured eye diagrams for (a) PIN Ge-PD at 1 V_{dc} and (b) Schottky Ge PD at 5 V_{dc} for 25 Gbps with 2^7-1 PRBS.

3. Results and discussion

Figure 2 shows (a) SEM image of selectively grown Ge with SiGe capping layers and (b) SIMS profile of Si and Ge in SiGe/Ge layers grown in optimized conditions [4]. By decreasing the SiGe growth temperature and reducing the H_2 flow rate, a smooth surface and an abrupt interface of SiGe/Ge were realized.

Figure 3 shows (a) photoresponsivity and (b) 3 dB bandwidth of the fabricated PIN and Schottky Ge PDs. Both Ge PDs showed good photoresponsivity of about 1.0A/W, and a low enough dark current density of 0.4 nA/μm^2 for the PIN Ge PD and 0.8 nA/μm^2 for the Schottky Ge PD. The frequency of the 3 dB bandwidth was 40 GHz for the PIN Ge PD and 30 GHz for the Schottky Ge PD. At lower DC bias voltage (V_{dc}), a much larger bandwidth was obtained for the PIN Ge PD. From the equivalent circuit model fitting, the Schottky Ge PD showed much larger capacitance around the zero bias voltage, which would show that the depletion layer thickness for the Schottky Ge PD was smaller than that of the PIN Ge PD.

Figure 4 shows measured eye diagrams for the PIN and the Schottky Ge PDs for 25 Gbps with a 2^7-1 non-return-to zero (NRZ) pseudo random binary sequence (PRBS). In this experiment, light from a 1.55-μm-wavelength laser was modulated and input into an external 30 GHz $LiNbO_3$ optical modulator at 25 Gbps. The clear open eyes suggest that the optical links are capable of 25 Gbps data transmission. Figure 5 shows the dependence of the 3 dB bandwidth for the Schottky Ge PDs on Ge thickness compared with that of the PIN Ge PD with 1-μm Ge thickness. A little improvement in the 3dB bandwidth was obtained for the 0.8-μm thickness of the Ge layer. On the other hand, the PIN Ge PD shows a larger bandwidth, which would originate

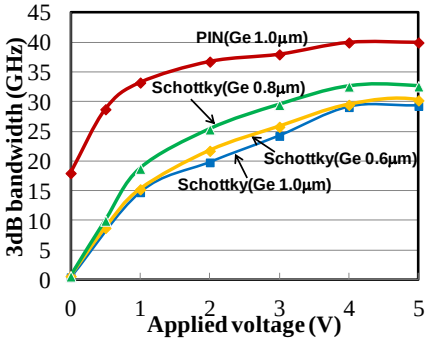

Fig. 5 Dependence of 3dB bandwidth for Schottky Ge PDs on Ge thickness compared with that of PIN Ge PD.

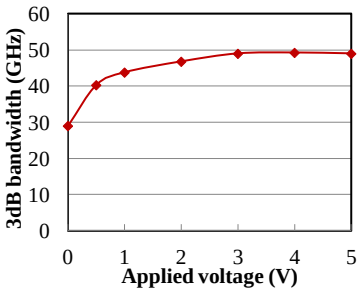

Fig. 6 3 dB bandwidth for the PIN Ge-PD on applied bias voltage with 0.6 μm thick Ge layer.

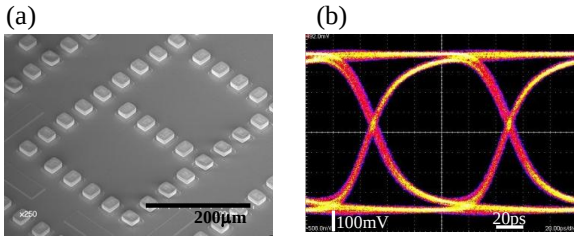

Fig. 7 (a) SEM image of CMOS TIA chip and (b) Output waveform from TIA linked with PIN Ge PD at 10 Gbps with -10 dBm average laser power.

from the smaller intrinsic Ge thickness due to P ion diffusion. In addition to the intrinsic Ge thickness, a carrier pileup at the SiGe/Ge interface may affect the 3dB bandwidth for the Schottky Ge PD [5]. Figure 6 shows the 3 dB bandwidth for the optimized PIN Ge PD on V_{dc} with a 0.6-μm thick Ge layer. An about 50 GHz bandwidth was obtained with a voltage more than 3 V_{dc}, and at even zero bias, 29 GHz bandwidth was obtained.

Finally, we studied a PIN Ge PD with a small footprint and low consumption CMOS TIA circuit. To achieve a smaller footprint and larger impedance gain, we used an inverter-type TIA circuit [6]. Figure 7 shows (a) SEM image of CMOS TIA chip and (b) output waveform from TIA linked with PIN Ge PD at 10 Gbps with a -10dBm average laser power. It achieved larger sensitivity than that of a conventional analog TIA circuit.

4. Conclusions

We studied the high performance of Si waveguide-integrated PIN and Schottky Ge PDs, which showed very low dark current density of 0.4-0.8 nA/μm^2 with a high efficiency of 1.0 A/W. A high speed of 50 GHz bandwidth was obtained for the optimized PIN Ge PD. We also reported on a PIN Ge PD connected to an inverter-type CMOS-TIA circuit, and 10 Gbps operation with high sensitivity was demonstrated.

Acknowledgements

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