Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp986-987

15 µm-pitch Cu/Au Interconnections Relied on Self-aligned Low-temperature Thermosonic Flip-chip Bonding Technique for Advanced Chip Stacking Applications

T. T. Bui,[1,2] F. Kato,[1] N. Watanabe,[1] S. Nemoto,[1] K. Kikuchi,[1] and M. Aoyagi[1,2]

[1] Nanoelectronics Research Institute (NeRI)
[2] Institute of Photonics-Electronics Convergence System Technology (PECST)
National Institute of Advanced Industrial Science and Technology
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568 Japan
Phone: +81-2-9862-6510 E-mail: m-aoyagi@aist.go.jp

1. Introduction

Continuous increase in demand for miniaturization and performance improvement of electronic products is well understood. We should promote the development of the Photonics and Electronics Convergent System Technology (PECST) [1] for heterogeneous multi chip integration in order to overcome the limitation of current LSI system technology. In realizing photonics-electronics heterogeneous integration systems, one obstacle is lack of a reliable method to stack optical device chips with LSI device chips, with high-accuracy at acceptable low temperature and low applying force. The technical challenge will attract the interest of many research groups who investigate advanced packaging technology, since it can offer higher interconnection density and performance.

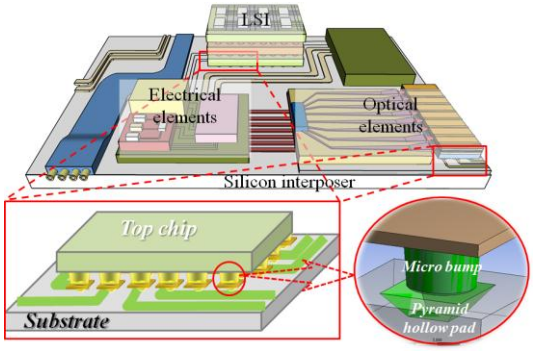

Fig. 1 Proposal of flip-chip bonding approach for advanced high-accuracy, fine-pitch chip stacking.

Flip-chip bonding (FCB) technique has been a promising technique for high density interconnection and heterogeneous integration. Though fine pitch interconnections are realized with micro bump technology [2], FCB still has the problem of the post-bond alignment shift causing the limit in the interconnection pitch. Attempting to improve the alignment accuracy of the FCB method through increasing the resolution of the alignment stage motion and increasing the magnification of the aligning camera is not sufficient. Additionally, a high-precision alignment system shows high cost and it requires very long processing time in actual production line. Self-alignment effects [3, 4], due to its high efficiency and high accuracy, should be introduced for advanced heterogeneous chip stacking applications.

In this paper, we present the results of fine-pitch bump interconnections using a modified flip-chip bonding approach [4], based on the self-alignment effect caused by misalignment self-correction elements (MSCEs), aiming to realize heterogeneous chip stacking with high-accuracy and fine-pitch interconnections.

2. Bonding approach and experimental procedure

The post bond accuracy in our work is improved by means of maintaining the alignment between the chip and substrate during bonding at acceptably low temperature by taking the advantages of thermosonic FCB utilizing of MSCEs. The MSCEs in this work constructed from electroplating bumps and modified bonding pads, i.e., anisotropic wet-etched inverted-pyramid (AWEIP) bonding pads (Fig. 1). The MSCEs offer both electrical connection and mechanical stacking functions. The bonding approach using of MSCEs is shown in Fig. 2. Under the application of an appropriate downward force, bumps are self-aligned with AWEIP pads, and the misalignment, which may have happened in the alignment process, is self-corrected and maintained at that state to the end of the bonding process.

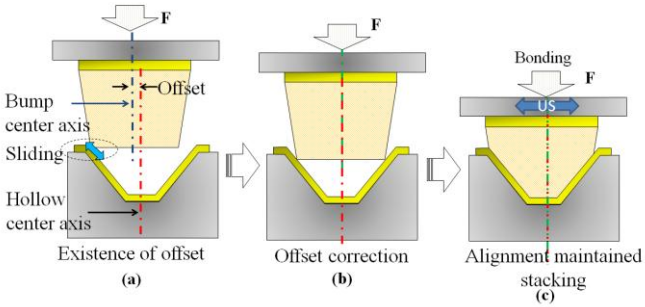

Fig. 2 Alignment maintained bonding approach using modified interconnection pair.

Table I Summary of bonding parameters.

Parameter	Value
Loading (gf/bump)	6
US amp. (µm)	2.2
US freq. (kHz)	48.5
Bonding time (s)	0.5
Bonding temp.	RT

The proposed bonding approach was applied to realize stacking chips with 15 µm-pitch microbump interconnections. Electroplating Cu bump and Au deposition AWEIP

pad are used as a MSCE pair. Reliable Cu-Au direct interconnection can be formed at room temperature with ultrasonic assisted bonding technology [5]. Si test chips were mounted onto Si substrates using a thermosonic flip-chip bonder (Table 1) in order to verifying the bonding approach. Cross-sections at bonding interface were also observed to confirm the deformation relationship of bump and conductive pad, as well as the formation of the bonds.

3. Experimental results and discussion

The fabricated test specimens and the bonded chip-substrate pair are shown in Fig. 3 and Fig. 4, respectively. Good I-V characteristic that was obtained from the daisy chain proved ohmic contacts of the microbump interconnections (Fig. 5). The proposed bonding approach was confirmed with the cross-sectional scanning electron microscopy (SEM) images shown in Fig. 6. Due to the presence of MSCEs, the offsets would be self-corrected and maintained during stacking and we succeeded in bringing to reality of repeatable chip stacking with 15 µm-pitch microbump interconnections.

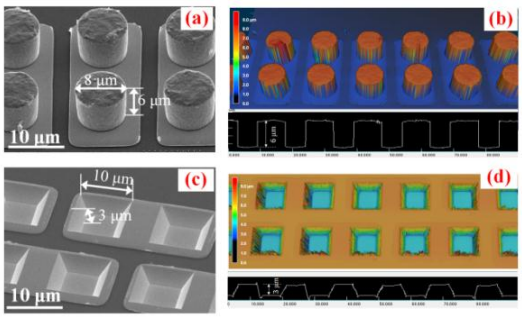

Fig. 3 Fabricated bumps and pads and their parameters.

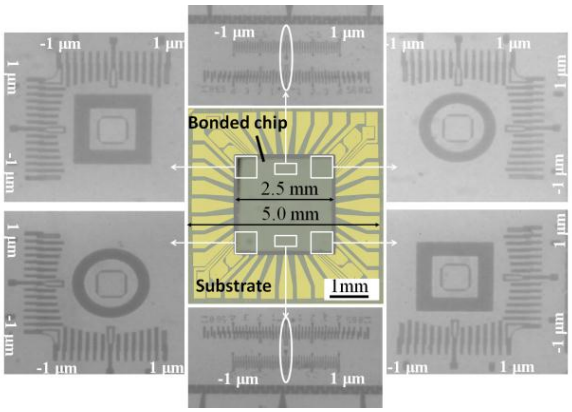

Fig. 4 Post-bonded offsets observed by an IR camera.

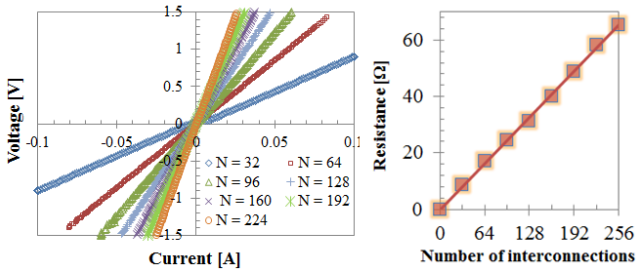

Fig. 5 Current-voltage characteristics of the daisy chain.

Fig. 7 shows a transmission electron microscopy (TEM) image at Cu-Au interface of the as-bonded chip for clarifying Cu bumps smoothly bonded onto Au bonding pads. The Cu-Au bond is successfully created at room temperature due to the ultrasonic assisted bonding technique and the presence of large friction force generated when the bumps get into the inverted pyramid bonding pads, resulting in a clean interface by removing surface contaminants.

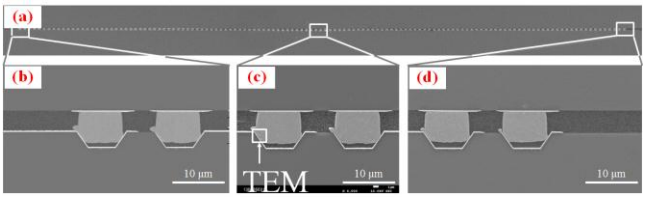

Fig. 6 Cross-sectional view at bonding interface.

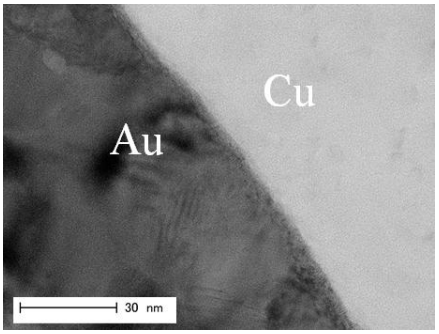

Fig. 7 Plane-view TEM images of bonded interface.

Moreover, with the proposed bonding approach, a high-accuracy alignment process is not required and conventional flip-chip bonders can be utilized, i.e. time efficiently and economically. In company with high alignment precision and low process temperature properties, the proposed bonding approach can be utilized in advanced device integration applications with requirement of precise assembly, and it contributes significantly to the development of PECST.

Conclusion

A bonding process using a modified bonding pad and an electroplated Cu bump was introduced. Experimental verification was implemented and stacking results were examined. We succeeded in bringing about reliable fine-pitch interconnections (i.e., ϕ8 µm-bump, 15 µm-pitch) using flip-chip bonding technique for applicable in advanced integration applications.

Acknowledgement

This research is granted by JSPS through the FIRST Program, initiated by CSTP.

Reference

[1] Y. Urino et. al., Opt. Express, **19**, p. B159, 2011.

[2] A. Yu, et.al., *Proc. ECTC*, 2009, pp. 6 –10.

[3] T. Fukushima, et. al., *Proc. IEEE 61st Electronic Component and Technology*, 2011, pp. 2050–2055.

[4] T. T. Bui et. al., Jpn. J. Appl. Phys, **52**, p. 04CB08, 2013.

[5] Y. Tian, et. al., J. Mat. Proces. Tech., **208**, p. 179–186, 2008.