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Self-Assembly Study to Precisely Align Dies Having Microbump Covered with Non-Conductive Film for Advanced Chip-to-Wafer 3D Integration

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Abstract

We demonstrated new self-assembly for high-throughput and high-yield multichip-to-wafer 3D stacking using chips covered with a non-conductive film (NCF) on the top surface. The NCF is a promising candidate to completely fill between small microbumps of the chips and is essential for realizing fine-pitch microbump-to-microbump interconnections. 3-mm-square chips laminated with the NCF were precisely self-assembled to wafers within 4 μm by surface tension of water. The results indicate that the self-assembly technique using chips with the NCF can achieve not only high-accurate chip alignment but also high-strength chip bonding at once.

1. Introduction

Chip-to-wafer integration is an attractive 3D integration method to realize high-production yield owing to the usage of known good dies (KGDs). In particular, advanced multichip-to-wafer method using self-assembly with liquid surface tension is a promising technique for 3D integration, which can also overcome trade-off between throughput and alignment accuracy in conventional mechanical assembly [1]. When we use chips with metal microbumps for multichip self-assembly [2-5], the chips are thermally compressed and interconnected to the corresponding wafers with metal microbumps. Then, an "underfilling" process with liquid resins using capillary force is required for injecting the resins into the resulting narrow gap between the chips and wafers in order to obtain highly-reliable microbump interconnections. However, as the gap and bump sizes/pitches recently become smaller and smaller, conventional capillary underfilling suffers from low throughput and void generation. Therefore, capillary underfilling is not suitable for chip-to-wafer 3D integration. NCF is often alternatively used for the capillary underfill resins and can be formed in wafer-level. In this paper, we propose new self-assembly using chips with metal microbumps covered with NCF for advanced chip-to-wafer 3D integration. Figure 1 shows chip self-assembly with NCF onto SiO_2 assembly areas on a wafer. Immediately after self-assembly and the subsequent thermal compression, NCF is ejected from the bump top to give microbump joining and underfilling is simultaneously completed. This method can skip bothering one-by-one underfilling processes after bump connection. Here, we demonstrate self-assembly with chips having NCF and evaluate alignment accuracies.

2. Experimental

Assembly wafers and chips used in this study were prepared from Si wafers with a hydrophilic SiO_2 layer and metallized vernier scales for alignment accuracy evaluation. In assembly wafer fabrication, hydrophobic fluorocarbon areas surrounding the hydrophilic assembly areas were patterned by lithography and lift-off processes. In chip fabrication, a NCF was laminated on a 140-μm-thick wafers by a vacuum laminator. After that, 3-mm-squire chips were diced by blade dicing with chip size accuracies within ±2.5 μm (hereinafter referred to as "NCF chip").

In self-assembly processes, we employed an industrial scalar robot to sort the chips from chip trays on which KGDs without dimensional errors and visible defects such as particles and scratches were arrayed. A 0.4 μl ultrapure water droplet was provided onto the hydrophilic assembly area on the assembly wafers, and then, the chips were roughly pre-aligned until the NCF surface was contacted to the water droplet. After keeping a 100-μm height between the chips and the wafers, the chips were released to the assembly areas. After spontaneous water evaporation, alignment accuracies of the assembled chips were evaluated by observing vernier pattern with an IR microscopy. For comparison, 140-μm-thick chips having a SiO_2 layer on the top surface and diced by plasma etching within ±2.0 μm (hereinafter referred to as "SiO_2 chip") were also evaluated. We have demonstrated self-assembly-based 3D integration [1-5], where multichip self-assembly with submicron accuracies can be given by the hydrophilic SiO_2 chips.

3. Results and Discussion

Size precisions of SiO_2 chips and NCF chips after dicing were 2999.0 ±2.0 μm and 2999.9 ±3.0 μm, respectively. The former size precision was influenced mainly by lithography, whereas the latter size precision was influenced by blade dicing. The NCF chips were rapidly assembled to the

assembly areas on the wafers by water surface tension as well as the SiO_2 chips. Figure 2 shows that a NCF chip with 500-µm-initial displacement swam to the assembly area for 0.27 sec. The NCF chips can be precisely assembled to the corresponding hydrophilic areas even by 1000-µm initial displacement, but that depends on self-assembly conditions such as chip release height, cleanliness on chips and wafers, water volume, robot sorting speed, and so on.

Figure 3 shows photomicrographs of vernier patterns after self-assembly. Figure 4 shows alignment position maps when we use 10 SiO_2 chips and NCF chips. Alignment accuracies for the SiO_2 chips were 0.9 µm on average and 2.0 µm at worst. In contrast, the NCF chips were aligned with an average accuracy of 2.8 µm and within 3.9 µm in the worst case. The NCF chips could be also successfully assembled with high alignment accuracy as well as the SiO_2 chips. The difference in alignment accuracies between both chips mainly derived from chip size precisions. In addition, slight NCF undulation and fractions peeling could be found on the dicing edge due to viscoelasticity of the NCF and less adhesion strength of the NCF to Si or SiO_2. However, the NCF chips provided good prospects to obtain higher chip alignment accuracy by optimization of chip fabrication processes.

4. Conclusions

We preformed fundamental studies of self-assembly with NCF chips by water surface tension to achieve micobump-to-microbump interconnections for advanced chip-to-wafer 3D integration. 3-mm-square NCF chips were self-assembled to hydrophilic areas formed on wafers within 2-3 µm. The alignment accuracies can further increase and we would realize higher alignment accuracies comparable to SiO_2 chips employed in our previous works using the NCF chips.

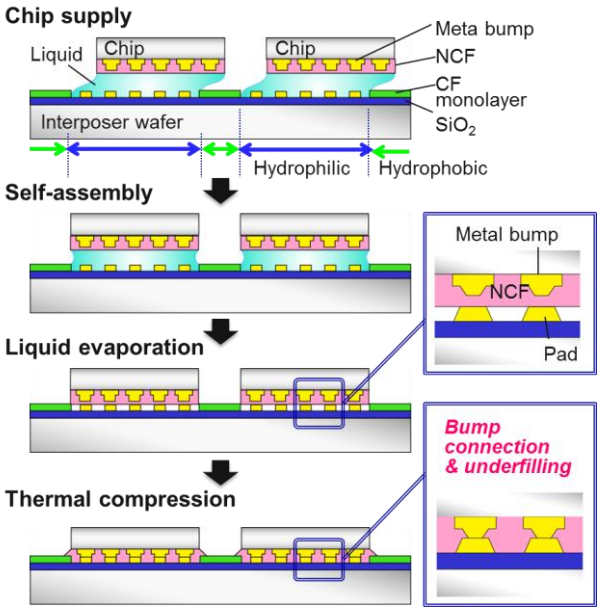

Fig. 1 Conceptual image of self-assembly using chips having metal microbump covered with NCF to the wafer.

References

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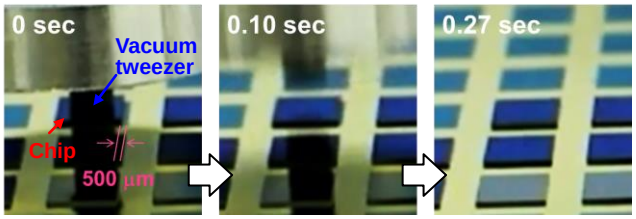


Fig. 2 Self-assembly behavior of a NCF chip to wafer by 500-µm-initial displacement captured with high-speed camera.

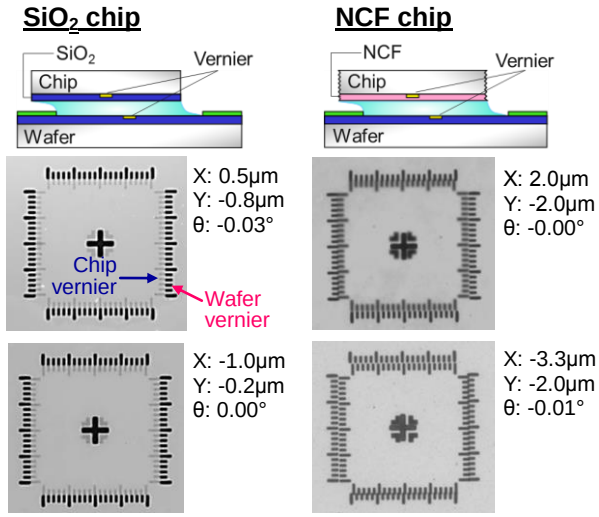
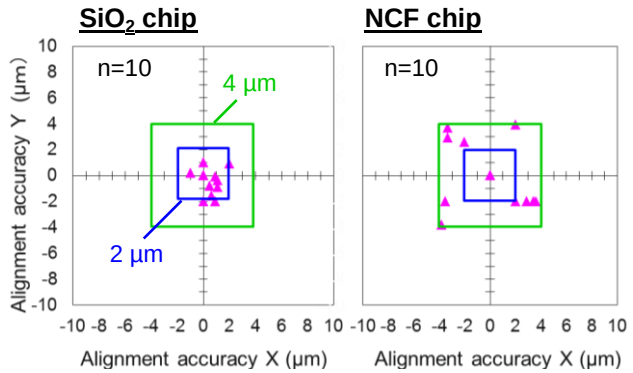


Fig. 3 Vernier images on SiO_2 chip (left) and NCF chips (right) through IR microscopy.



	SiO_2 chip			NCF chip		
(µm)	|x0|	|y0|	|θ|	|x0|	|y0|	|θ|
Ave.	0.81	0.99	0.01	2.98	2.69	0.01
Max.	2.0	2.0	0.03	3.8	3.9	0.03
Min.	0.0	0.1	0.0	2.0	2.0	0.0
S.D.	0.58585	0.68548	0.01048	0.71461	0.82657	0.01048

Fig. 4 Alignment position maps between SiO_2 chips without NCF (left) and NCF chip (right).