Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp1008-1009

Optical modulation based on surface plasmon resonance using metal-insulator-semiconductor structure

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Abstract

A silicon optical modulator based on surface plasmon resonance is demonstrated theoretically and experimentally. This device has metal-insulator-semiconductor structure on silicon channel waveguide. The extinction ratio of 1.6 dB at gate voltage 1.3 V is obtained experimentally.

1. Introduction

Silicon photonics has been researched with the aim of realization of silicon based micro-optical circuits and optical interconnection of large-scale integrated circuits. Silicon optical modulator is one of important devices for silicon photonics. Silicon optical modulator for on-chip optical interconnection [1-5] has to meet various requirements such as high-speed modulation, large extinction ratio, low power consumption, compact device size, and so on. But it is difficult to meet these all requirements. With the goal of meeting these all requirements, we propose a novel silicon optical modulator based on surface plasmon resonance [6]. This device has a metal-insulator-semiconductor (MIS) field effect transistor structure as shown in Fig. 1. Intensity of the light propagating through the waveguide is controlled by the surface plasmon resonance caused by the applied gate voltage. In this paper, we demonstrate the light modulation of proposed modulator by theoretical analysis and experimental.

2. Modulation Mechanism

The modulation mechanism of our proposed modulator is shown in Fig. 2. The input light propagates through the silicon-on-insulator (SOI) core while repeating total internal reflections. When applying a bias voltage to the polysilicon gate electrode, the inversion (or accumulation) layer which is filled with high concentration free carriers is formed. Since the inversion (or accumulation) layer behaves like a metal thin film, it is expected that the guided waves interact with surface plasmons at the interface of the inversion layer and gate oxide film at a particular bias voltage. The light coupled with the surface plasmon loses energy because part of light energy moves to the surface plasmon. As a result, the power of the output light decreases.

3. Device fabrication

The proposed modulator on SOI wafer can be fabricated with silicon CMOS compatible process. Firstly, waveguide patterns were made by electron beam lithography and reactive ion etching. Next, n^+ regions for source and drain were formed by implantation of phosphorous ions. The gate insulator was made of silicon nitride (Si_3N_4) in 10 nm thickness by using low pressure chemical vapor deposition (LPCVD). Gate electrodes were made of polysilion by LPCVD, and phosphorous ions were doped. Gate electrode patterns were formed by electron beam lithography and etchant (2.5% aqueous solution of tetramethylammonium hydroxide). Non-doped silicate glass (NSG) and phosphosilicate glass (PSG) layers were deposited by atmospheric pressure chemical vapor deposition and then Al electrodes were formed.

4. Result and Discussion

Figure 3 shows calculation results of the dielectric constant of the accumulation and inversion layer in p-type silicon when the gate voltage is applied. The flat band voltage is ignored for simplicity. It is confirmed that the dielectric constant becomes negative when a large bias voltage applied. It is one of the necessary conditions for causing surface plasmon resonance that the dielectric constant of metal film becomes negative.

Figure 4 shows calculation results of gate voltage dependence of the propagation loss for TM-like mode of the proposed modulator with various core thickness T and fixed width W = 800 nm. The thickness T_{SiN} of gate insulator (Si_3N_4) is fixed to 10 nm. In this paper, the wavelength of input light is fixed to 1540 nm. The feature of optical modulation by surface plasmon resonance is that the optical absorption appears as a sharp dip at a certain voltage. On the other hand, propagation losses slowly increase when the applied gate voltage becomes large. This is due to free carrier absorption in inversion or accumulation layer [7]. From these figures, the propagation loss by surface plasmon resonance becomes large if reducing the size of the waveguide. When the waveguide core thickness is set to around 500 nm, very large propagation loss is obtained.

Figure 5 shows the cross sectional SEM image of the fabricated modulator. The waveguide core is 533 nm in thickness and 767 nm in width. The gate insulator thickness is 10 nm. The flat band voltage is around -2 V as shown in Fig. 6.

Figure 7 shows the gate voltage dependence of the output light intensity from the fabricated modulator having gate electrode of 100 μm in length when TM polarized wave inputted. The output light intensity decreases significantly when the gate voltage is about 1.3 V and the drain voltage V_d is 0 V. As the drain voltage increases, the extinction ratio is reduced. This reason is considered that a pinch-off point appears and the length of effective channel (inversion layer) reduces when a large drain voltage is applied.

3. Conclusions

We demonstrated a silicon optical modulator based on surface plasmon resonance by theoretical analysis and experimental. The extinction ratio of 1.6 dB at gate voltage 1.3 V is obtained by the fabricated modulator with 100 μm gate length. The optical modulation can be improved by optimizing the core thickness and width of modulator.

Acknowledgements

This work was partly supported by a Grant-in-Aid for Scientific Research (C) (No.23560399) from the Japan Society for the Promotion of Science.

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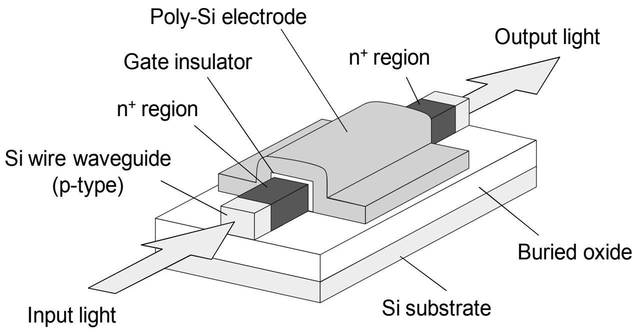

Fig. 1 Schematic structure of proposed optical modulator which has an MIS structure on SOI wafer.

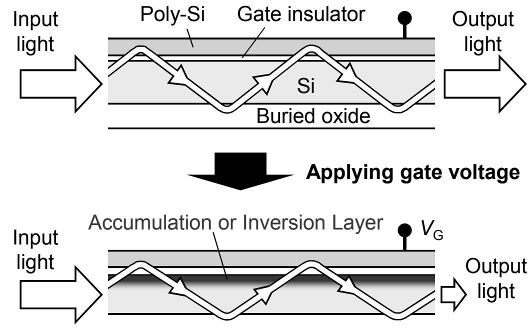

Fig. 2 Modulation mechanism of the proposed modulator. When applying a bias voltage, the inversion or accumulation layer appears. Since the inversion or accumulation layer behaves like a metal film, the guided waves interact with surface plasmons at a particular bias voltage.

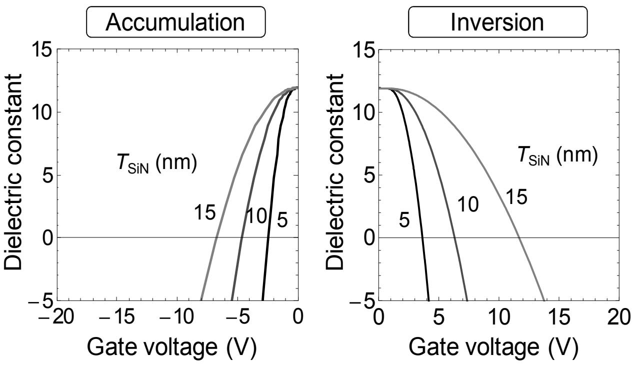

Fig. 3 Dielectric constant of accumulation or inversion layer vs. applied gate voltage. T_{SiN} denotes the thickness of the gate insulator film (Si_3N_4).

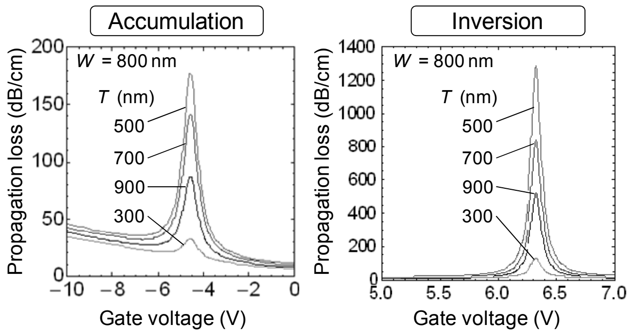

Fig. 4 Gate voltage dependence of propagation loss of TM-like mode for the proposed modulator.

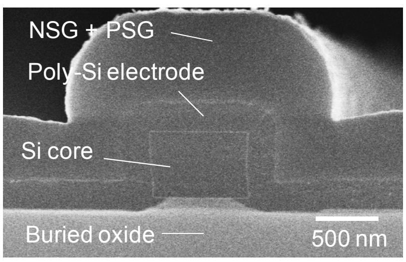

Fig. 5 Cross sectional SEM image of the fabricated modulator.

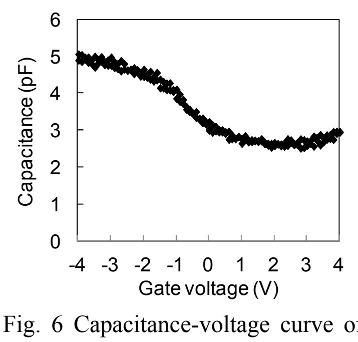

Fig. 6 Capacitance-voltage curve of the fabricated device under test.

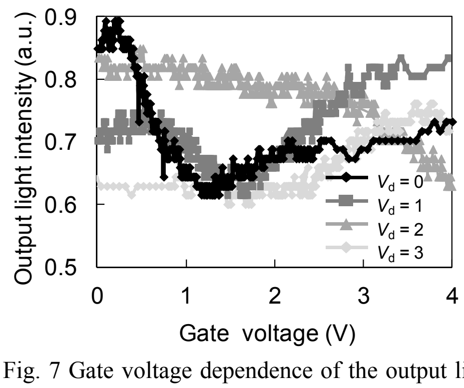

Fig. 7 Gate voltage dependence of the output light intensity from the fabricated modulator having gate electrode of 100 μm length when inputting TM polarized wave with wavelength 1540 nm.