600 V-class Trench-Filling Super Junction MOSFET for High precision processing technology

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1. Introduction
The Super Junction (SJ) MOSFETs are known to improve the trade-off between breakdown voltage and specific on-resistance (RonA). In SJ MOSFETs, the drift region has a structure that p- and n- columns aligned alternately. The higher aspect p/n columns obtain the lower RonA. Though several techniques to fabricate p/n column structures have been reported, the trench filling epitaxial growth technique is most simple and suitable for making a high aspect ratio p/n column structure [1]-[3]. The fabrication of the p/n columns in trench filling technique consists of three processes, deep trench formation in the n-type epitaxial layer, trench refilling by the epitaxially grown p-type layer and chemical-mechanical planarization (CMP) removal of the excess p-type layer. With the high aspect ratio structure, the MOSFETs characteristics are strongly influenced by process variation theoretically. The p/n column thickness greatly affects the breakdown voltage, and high-precision thickness control is especially required. Thickness control using the polish stop layer is widely used. In this method, the CMP stops at a stopper layer such as SiO₂ for different material removal rate selectivity. While epitaxial growing, however, surface protrusions and crystal defects are generated by overgrowth from the interface between the silicon and SiO₂ (Fig. 3). These defects cause functional degradation as leakage current. Therefore, it is desirable for the stopper SiO₂ layer to be left except the column region.

In this work, we report a self-align technology, in which the SiO₂ layer only in the column region removed. Optimized H₂ annealing realizes such selective patterning. And electrical properties of the SJ MOSFET fabricated with this technology are also revealed.

2. Results
Fig. 4 shows the cross-sectional SEM image after H₂ annealing for patterned SiO₂ on the n-type epitaxial layer (H₂ annealing temperature is 1170 degrees C, and processing time is 2, 5 and 10 minutes). While the SiO₂ thickness is hardly changed even when extending the processing time, the lateral recession is larger with time. SiO₂ layer seems almost completely diminished after 10 minutes.

Fig. 5 compares the “vertical etch rate” and the “lateral etch rate” of SiO₂ with respect to H₂ annealing time. The lateral etch rate was about 360 times faster than the vertical etch rate. The following chemical reaction Eq. (1) is generally known as a reduction of SiO₂ in the H₂ annealing [4]. SiO₂ is etched due to the formation and sublimation of silicon monoxide.

\[ SiO₂ + H₂(g) → SiO(g) + H₂O(g) \]  (1)

However, this reaction cannot describe the difference between the vertical and the lateral etch rate. We assume this reaction occurred specifically at the interface of SiO₂ and Si. Lee [5] reported for the reaction at the interface between Si and SiO₂, as shown in the following equation.

\[ Si – H + SiO₂ → Si⁺ + H₂O(g) \]  (2)
\[ Si⁺ + SiO₂ → SiO(g) \]  (3)
\[ Si + 2H₂O(g) → SiO₂ + 2H₂ \]  (4)

In Eq. (2), H attached on Si react with SiO₂ to yield water vapor (H₂O) and adsorbed silicon (Si⁺). These silicon atoms are prone to react with silicon dioxide to form volatile SiO₂. Some of the water vapor re-oxides the exposed silicon to form silicon dioxide. As shown in Eq. (3) and (4), both Si and SiO₂ are consumed at the interface. Therefore, we estimate that the SiO₂ etching is accelerated at the interface between the Si and SiO₂.

Fig. 6 shows the process flow of the SJ MOSFET with this technology. At first, SiO₂ layer deposited on the n-type epitaxial layer is patterned as a hard mask for subsequent silicon etching. Next, deep trenches are formed. Then, the SiO₂ layer only on the n-type column is removed by H₂ annealing. Annealing condition of 1170 degrees C, 10 minutes, SiO₂ layer will be approximately 3.2 μm recession. This is nearly equivalent to the column width. Therefore, the SiO₂ layer on the n-type column would be disappeared by etching from both sides. Meanwhile, since the peripheral width of the chip is about 100 μm, the SiO₂ remains enough. As a result, it is possible to produce the desired structure without the use of photolithography. After that, trench columns are filled by p-type epitaxial growth. Finally, the excess p-type layer is removed by CMP. The CMP is stopped at the remaining SiO₂.

Fig. 7 shows the surface optical photographs before and after H₂ annealing. The SiO₂ in the column region has disappeared after H₂ annealing, and the other has left.

The depth of trench after CMP is exhibited in Fig. 8. The variation was improved 12% to 2.5%.

Similarly, the variation is reduced to 8% from 20% for the breakdown voltage, as shown in Fig. 9.

3. Conclusion
We have developed a precise polishing method using a new SiO₂ patterning technology by H₂ annealing. Accuracy is improved about 5 times the control of depth, variation of breakdown voltage was reduced 60%.

4. References
Fig.1 Schematic of a SJ-MOSFET

Fig.2 Schematic process flow of SJ-MOSFET

Fig.3 Cross-sectional images of the crystal defects generated by overgrowth from the interface between the silicon and SiO2 (SEM)

Fig.4 Surface and cross-section image after H2 annealing (SEM)

Fig.5 Relationship of SiO2-etching to the processing-time of H2 annealing

Fig.6 Schematic new process flow of a SJ-MOS

Fig.7 Surface image of SJ-MOS in a new process

Fig.8 Comparison of trench depth (after CMP)

Fig.9 Comparison of Vd-Id waveform