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Impact of Silicon on Diamond Structure for Power-Supply on Chip Applications

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Abstract

This paper assesses Silicon-on-diamond (SOD) structure compared to the conventional SOI for Power-SoC applications. The SOD has thermal advantages over the conventional SOI without degrading electrical characteristics even using thinner diamond film (0.3 μm).

1. Introduction

Recently, power supply on chip (power-SoC) have been attracted attentions of many researchers because it can realize ultimate minimization of the power supply[1]. One of the effective ways to shrink the size of the power supply is to reduce the volume of the passive components such as inductors and capacitors. Increasing the switching frequency of power supply is one of the most promising approaches to do this. In such a scheme, SOI technology is one of the promising candidates for realizing power-SoCs, because it has inherent advantages of smaller parasitic capacitance than conventional bulk technology, which enable to fast switching performance, and devices completely isolate each other[2]. However, SOI technology has a problem of self-heating because of poor thermal conductivity of SiO_2. The silicon on diamond substrate(SOD), which uses thin diamond film used as an insulator to improve thermal conductivity of the substrate, is attractive because low high thermal conductivity of the insulating diamond film[3]. However, for power SoC applications, it is important to realize good thermal dissipation without degrading breakdown voltage.

This paper investigates impact of SOD structure for thermal property and device performance based on numerical simulations.

2. Device structure and material constants

The schematic cross section of the simulated SOD structure is shown in Fig. 2. A material constant used in this simulations are listed in Table.1. We used diamond film for a buried insulator and a surface insulating film. The thickness of the insulator was set by consideration of target breakdown voltage (in this case 30 V). cm^{-3}

3. Result & Discussion

Dependence of the highest temperature of the SOD on active Si layer thickness is shown in Fig. 3. The result of the conventional SOI is also shown in this figure. In this simulation, we consider only heat conduction and give amount of heat which is correspond to keeping temperature of 400 K for the active silicon layer of the conventional SOI structure. The maximum temperature decreases as decreasing top Si layer thickness. When the thickness of the active layer is 0.15 μm, the highest temperature of the active Si layer is reduced 40 K even at the 0.3 μm-thick diamond film. The reduction of the temperature for the

Table.1 Material constants used in simulations

Parameter	Si	SiO_2	Diamond	Air
Specific heat [J/kg/K]	700	780	520	1000
Density [kg/m^3]	2330	2200	3500	1.2
Thermal conductivity [W/m/K]	145	1.4	20	0.026

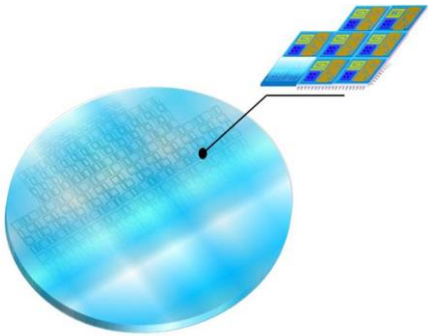

Fig.1 Power-SoC.

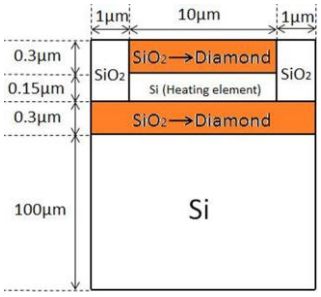

Fig.2 Schematic cross section of simulated structure.

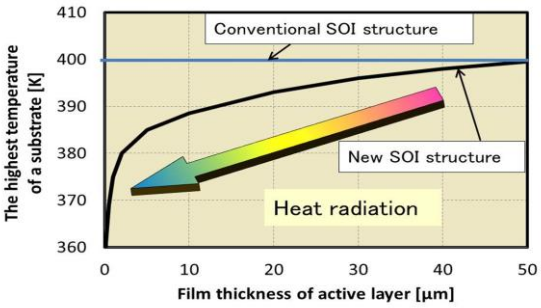

Fig.3 Dependence of the temperature of the active Si layer on the active Si layer thickness

active Si layer of 40 K increases the breakdown voltage of 4 - 5 V and reduces the on-resistance of approximately 5 % from the results of high temperature device characteristics of the 30V-class thin-film SOI power MOSFET[4].

Dependence of the highest temperature for active Si layer of SOD on the thermal conductivity of diamond film is shown in Fig. 4. In this simulation, the conditions are the same for Fig. 3. The highest temperature increases with decreasing thermal conductivity. The reduction in the highest temperature of SOD compared to the conventional SOI structure is 40K when the thermal conductivity of the diamond film is even at 20 W/m/K. The reduction in highest temperature of another SOD structure whose insulating diamond film is only buried insulator is 23K at the thermal conductivity of the diamond film is even at 20 W/m/K. The thermal conductivity of nano-crystalline diamond formed by plasma enhanced CVD is 20 W/m/K[5]. The surface roughness of nano-crystalline diamond is sufficient (Fig.4 Photo[4].) for wafer direct bonding process when we fabricate SOD substrate.

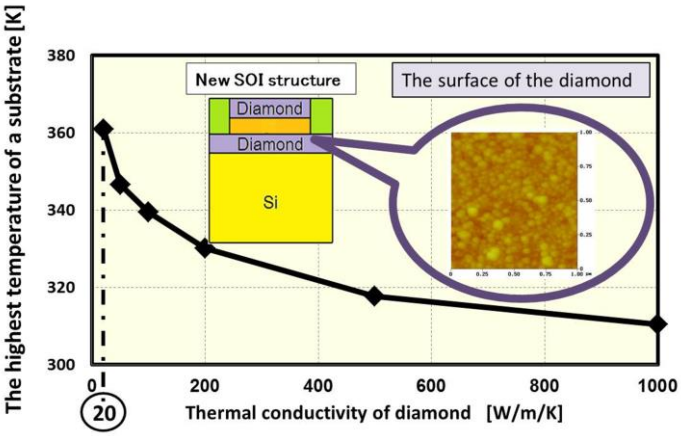

Fig.4 Thermal conductivity change of the diamond

Dependence of the breakdown voltage on the impurity concentration in drift region obtained by 2D-device simulation is shown in Fig. 5. The breakdown voltage of the SOI power MOSFET is slightly higher, however there is no problem in operations as 30V-class MOSFET.

Fig. 6 shows the transient thermal response for the power

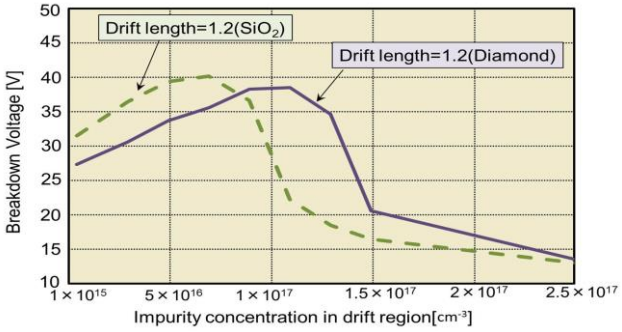

Fig. 5 Dependence of breakdown voltage on impurity concentration of the drift region

MOSFET fabricated on SOD compared to that for fabricated on the conventional SOI substrate obtained by 2D-device simulation. The switching frequency is 1MHz and duty ratio is 0.5. The highest temperature for both MOSFETs rise as time has elapsed. The highest temperature of the power MOSFET fabricated on the SOD is lower than that of power MOSFET fabricated on the conventional SOI substrate.

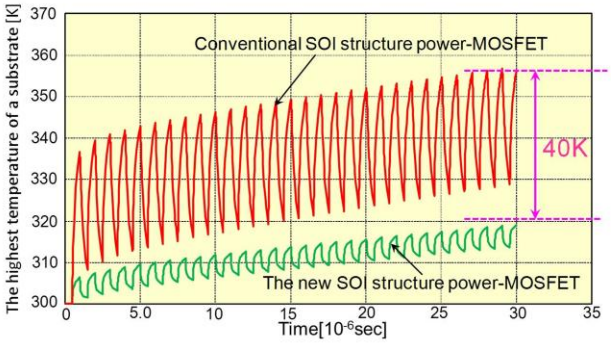

Fig.6 Transient temperature response of the SOI power-MOSFET

4. Conclusions

We evaluate the SOD substrate compared to conventional SOI one for power-SoC applications. The SOD substrate showed good heat dissipation without degrading electrical performance.

Acknowledgements

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