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Micro Dynamic Avalanche Phenomenon during Turn-off in Si-IGBTs

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1. Introduction

It is well known that the turn-off surge of silicon IGBTs decreases with small gate resistance, in contrast to MOS devices. In this gate resistance region, the turn-off loss is reduced, but at the same time the turn-off di/dt can not be controlled by the gate resistance. Therefore, the clarification of these phenomena in this region based on the device's physics has been strongly required to expand its applications. However, limited information is available on the relationship between gate resistance and turn-off surge [1].

In this study, the dependence of the turn-off surge on gate resistance and temperature were investigated. It was confirmed that the surge decrease with small gate resistance derives from a dynamic avalanche phenomenon adjacent to the bottom of the trench. In addition, it was found that this surge decrease is affected even by a smaller avalanche generation rate (micro dynamic avalanche) compared with that in a critical electric field.

2. Experiments

In order to evaluate the gate resistance (R_G) and temperature dependences of the turn-off surge (V_{SG}), a commercial 1.2kV /30A trench IGBT and PiN diode were prepared. The switching waveforms of R_G and temperature for each were measured with an inductive load. The dependence of V_{SG} on R_G and temperature was measured by adjusting the external resistance connected to the gate driver and the temperature of the hot plate, respectively.

3. Results and Discussion

Figure 1 shows the measured R_G dependence of V_{SG} at various temperatures. V_{SG} increased as R_G decreased from 150 to 60 ohms. However, V_{SG} was at its maximum value around 60 ohms and decreased with smaller R_G. In this work, we defined the regions of surge decrease and increase with decrease in R_G as Regions I and II, respectively, as depicted in Figure 1. In Region I, V_{SG} increased with elevated temperature. However, V_{SG} was almost independent of the temperature in Region II. Figure 2 shows a simulated R_G dependence of V_{SG} with temperature. The simulated results are similar to the measurements.

To clarify the origin of the surge decrease in Region I, the internal dynamics of the IGBT during turn-off were investigated. Figures 3 and 4 show the simulated switching waveforms in Regions I and II, respectively. The time evolution of the carrier concentration, space charge, and avalanche generation rate (G_A) adjacent to the bottom of trench are also shown. In Region I, rapid increase in the positive space charge, carrier concentration, and G_A occurs at the collector current turn-off (t_{OFF}). This behavior during turn-off does not occur in Region II.

These simulated results indicate that the dynamic avalanche is generated adjacent to the bottom of the trench. Figure 5 shows the dependence of V_{SG} and G_A at t_{OFF} with R_G and temperature. G_A in Region II is very low. Meanwhile, G_A in Region I increases drastically with decrease in R_G and temperature. This temperature dependency may be caused by the activation of lattice vibration. The decrease of G_A with temperature corresponds well with the temperature dependence of V_{SG}.

From the above analysis, strong correlations between V_{SG} and G_A with R_G and temperature were found. Next, the origin of the surge decrease will be considered. Figure 6 shows a schematic diagram of the internal space charges at different regions at t_{OFF}. At this time, the maximum electric field (E_{max}) near the bottom of the trench is mainly determined by the amount of the net space charge $Q=N_D+p-n$, where N_D, p, and n are the donor, hole, and electron concentration, respectively. In the case of Region I, the electron injection via the MOS channel into the depletion layer is negligible ($n\approx0$) because the gate-emitter voltage is lower than the threshold voltage (V_{th}) at t_{OFF} (see Figure 3). In Region II, on the other hand, the MOS channel is still open and thus supplies electrons to the depletion layer ($n>0$). As a result, E_{max} in Region I becomes higher than that in Region II due to the increase in the positive space charge. Thus, in Region I, the dynamic avalanche occurs more readily which causes a decrease in the surge.

Many studies have been reported previously on the self-clamping of the collector-emitter voltage caused by the dynamic avalanche phenomenon during turn-off [2-3]. In these cases, E_{max} reaches the critical electric field. In our case, the avalanche generation rate adjacent to the bottom of the trench when it reaches a critical electric field (G_{A_crit}) was estimated to be 0.6×10^{25} $cm^{-3}s^{-1}$ at T=300 K. Note that G_A in Region I is lower than G_{A_crit} as shown in Figure 5. This means that surge decrease can occur even when $G_A<G_{A\_crit}$; this is because a so-called "micro" dynamic avalanche. The avalanche generation rate plays a crucial role in V_{SG} especially with the small R_G.

4. Conclusions

In conclusion, the dependence of the turn-off surge on gate resistance and temperature were studied. From the measured and simulated results, it became clear that surge decrease can be attributed to a dynamic avalanche adjacent to the bottom of the trench. It was also found that even a small avalanche generation rate cause a surge decrease.

References

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[2] T. Ogura *et. al.*, Electron Devices, Vol. 51, pp. 629, 2004.

[3] M. Tsukuda *et. al.*, Proc. ISPSD'08, pp. 185, 2008.

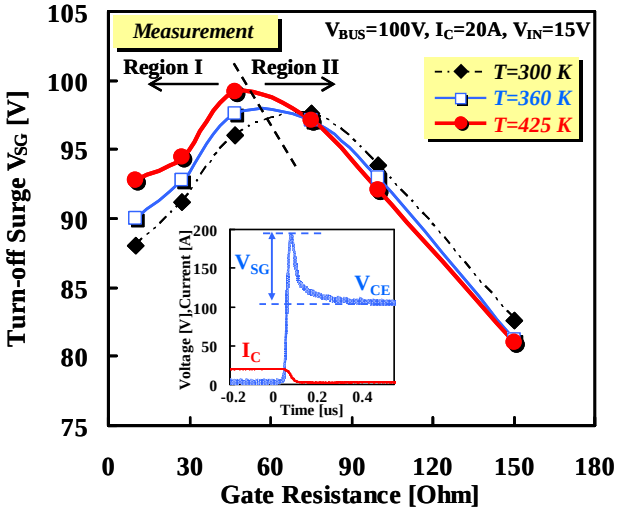

Fig. 1 Measured dependence of turn-off surge on gate resistance and temperature. Inset: Measured switching waveforms.

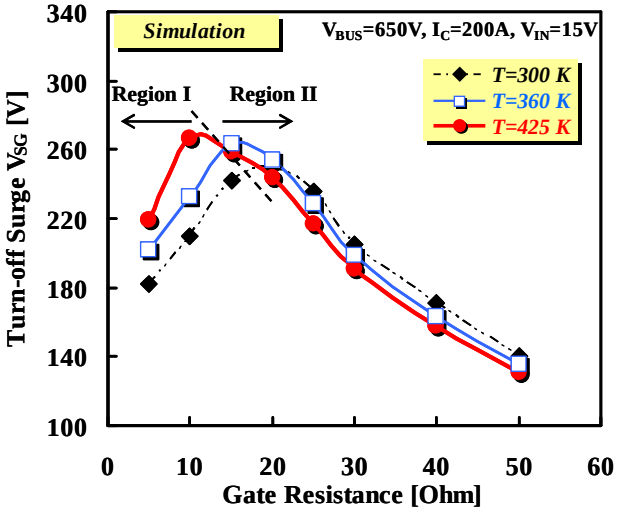

Fig. 2 Simulated dependence of turn-off surge on gate resistance and temperature.

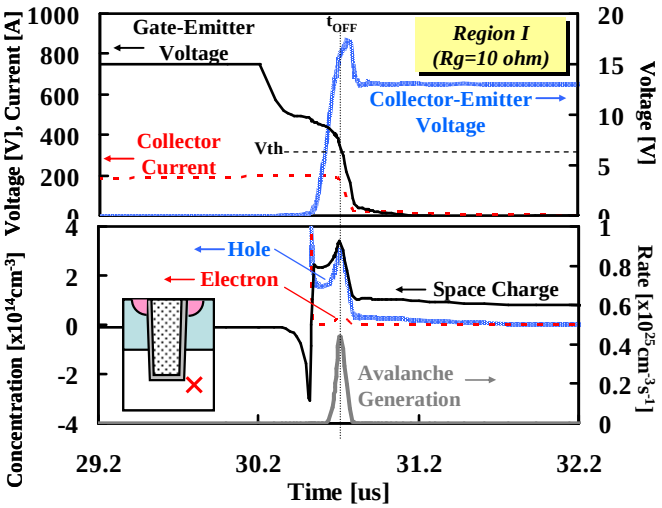

Fig. 3 Simulated switching waveforms and internal dynamics adjacent to bottom of trench for Region I.

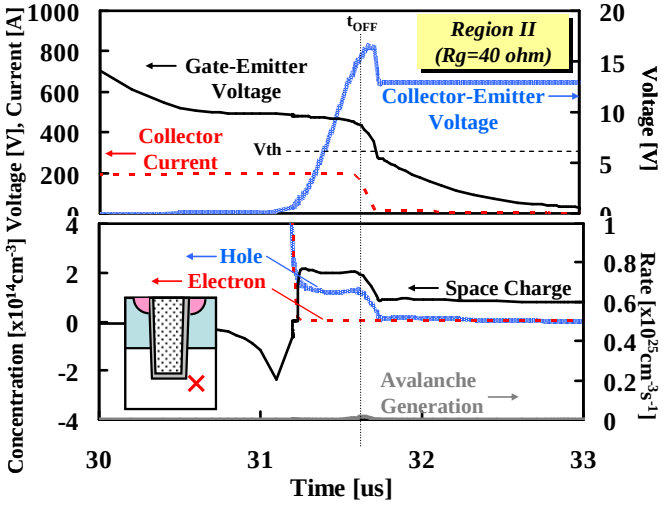

Fig. 4 Simulated switching waveforms and internal dynamics adjacent to bottom of trench for Region II.

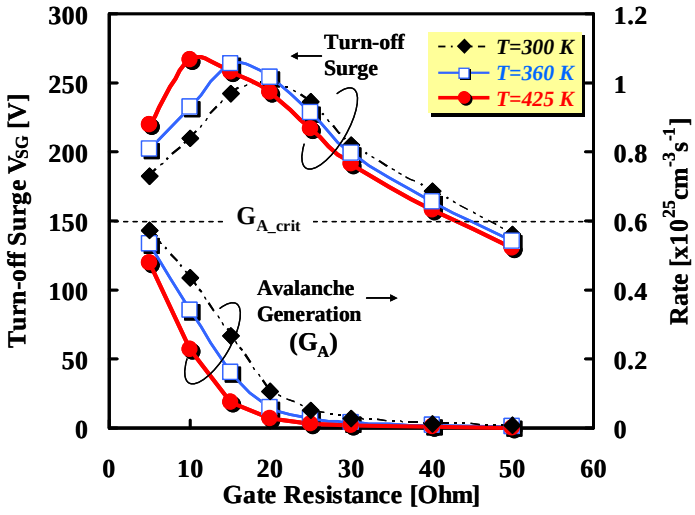

Fig. 5 Simulated dependence of turn-off surge and avalanche generation rate on gate resistance and temperature.

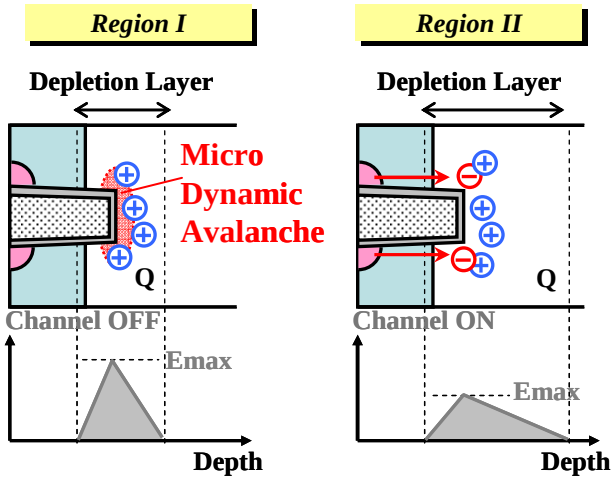

Fig. 6 Schematic diagram of internal space charges at each region just before collector current turn-off.