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Suppression of Reverse Recovery Surge Voltage of Silicon Power Diode by Adjusting Trap Energy Levels through Local Lifetime Control

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Abstract

To suppress reverse recovery surge voltage of silicon power diodes, effects of trap energy levels adjusted through local lifetime control were investigated. It was found that a deep trap energy level reduced surge voltage at 1000A/cm^2 or less current density regions.

1. Introduction

Suppression of the reverse recovery surge voltage of silicon diodes is being investigated, because this surge voltage causes EMI noise. In order to realize suppression of the surge voltage, optimization of excess carrier distribution by local lifetime control [1] and backside laser annealing [2] has been pursued.

Local lifetimes are formed by localizing traps where recombination takes place. Generally, the optimum position for the minimum lifetime is close to the anode junction. Therefore, the larger the ratio between the lifetime at the anode side and that at cathode side, the more the surge voltage is suppressed.

In addition, the reverse recovery characteristics also have an influence on trap energy levels. We verified that variations in recombination rate due to trap energy levels have an influence on the surge voltage [3]. Thus, through adjustment of trap energy levels, control of local lifetime may have a suppression effect on the surge voltage.

In this study, we investigated the effect of lifetime control on suppression of surge voltage through adjustment of trap energy levels, and developed guidelines for achieving suppression the surge voltage through the design of the silicon power diodes

2. Model and Equation

Figure 1 is a pattern diagram of the $P^+N^-N^+$ diode investigated in this study. The maximum trap density N_{t1} is ten times higher than the minimum trap density N_{t2}. The carrier lifetime τ_1 and τ_2 is dependent on trap energy levels as well as the trap density.

Under a high injection condition, the relationship between excess carrier density p_n, recombination rate R_r with various trap energy levels and carrier lifetime τ_p in the N-region can be established using the SRH model as follows [4]

$$R_r = \frac{\sigma v_{th} N_t p_n^2}{2\left[p_n + n_i \cosh\left\{\left(E_t - E_i\right)/kT\right\}\right]} + \frac{p_n}{\tau_{bulk}} = \frac{p_n}{\tau_p} \quad (1)$$

where σ is the capture cross section, v_{th} is the thermal velocity, N_t is the trap density, and τ_{bulk} is the intrinsic carrier lifetime in the bulk silicon substrate.

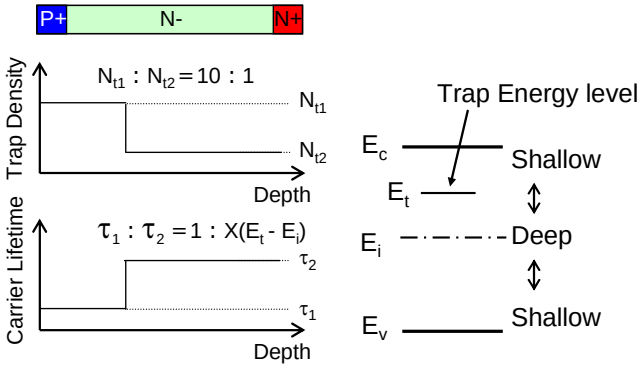

Fig. 1 Structure of $P^+N^-N^+$ diode and band diagram

3. Results and Discussion

Figure 2 shows the correlation between the recombination rate and the excess carrier density calculated with Eq.1, in the cases where Et-Ei=0.1eV (deep) and Et-Ei= 0.4eV (shallow).

Note that the slope of the Et-Ei=0.1eV line is constant whereas that of the Et-Ei= 0.4eV line varies with carrier density. This difference is caused by the difference in carrier emission probability from the trap. This is expressed by the term $n_i \cosh\left\{\left(E_t - E_i\right)/kT\right\}$ in Eq.1.

This term increases exponentially with the Et-Ei value. At the deep energy levels, Et-Ei is small, and the value of that term is negligible. In this case, Eq.1 can be approximated as follows.

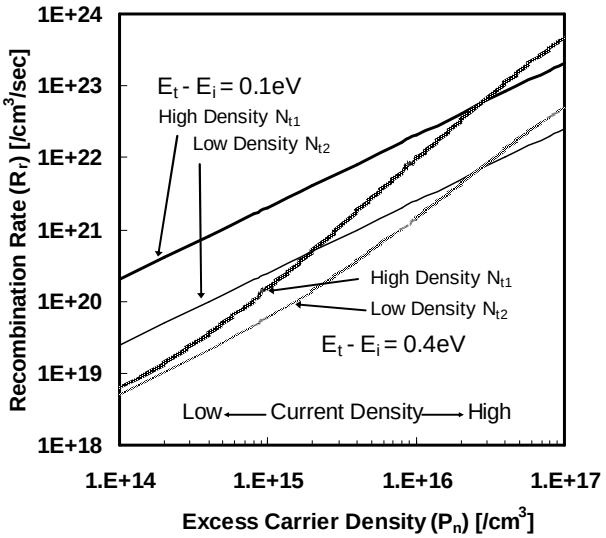

Fig. 2 Calculated correlation between recombination rate and excess carrier density (T=300K)

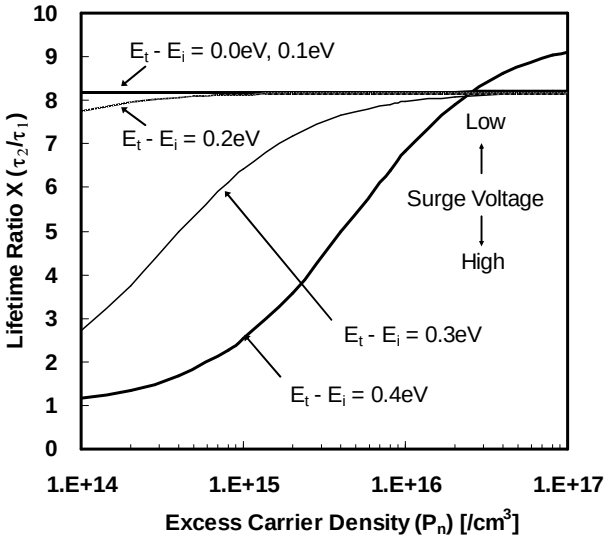

Fig. 3 Calculated correlation between lifetime ratio and excess carrier density with various trap energy levels (T=300K)

$$R_r = \frac{\sigma v_{th} N_t p_n}{2} + \frac{p_n}{\tau_{bulk}} \qquad (2)$$

Eq.2 indicates that the recombination rate is proportional to the excess carrier density and the trap density. With a particular difference in trap density, the difference in recombination rate is constant at any given excess carrier density. On the other hand, shallow trap energy levels do not maintain the same difference in recombination rate because of the high emission probability.

Figure 3 shows the relationship between the lifetime ratio τ_2/τ_1 and the excess carrier density, calculated from Eq.1. The larger the lifetime ratio, the larger the carrier density is at the anode side than at the cathode side, which suppresses the surge voltage. With deep trap energy levels such as Et-Ei= 0.0~0.2eV, the same lifetime ratio is maintained at any excess carrier density. With shallow trap energy levels such as Et-Ei= 0.3~0.4eV, the lifetime ratio varies greatly. With low or middle level excess carrier density, the lifetime ratio is higher with deep energy levels than shallow energy levels. With high excess carrier density, the lifetime ratio is lower with deep energy levels than shallow energy levels. This trend indicates that the surge voltage is lower at deep energy levels in low and middle current regions, and lower at shallow energy levels with high current.

Figure 4 shows simulated dependence of the surge on current at various trap energy levels. At 1000A/cm^2 or less, the surge voltage is lower with deep energy levels such as Et-Ei= 0.0~0.2eV. On the other hand, at over 1000A/cm^2, the surge voltage is the lowest when Et-Ei=0.4eV. This trend matches that shown in Fig.3. Shallow energy levels suppress surge voltage only when there is very high current. Thus, deep energy levels such as Et-Ei= 0.0~0.2eV are favorable for almost all power devices.

Figure 5 is a pattern diagram of trap energy levels created by local lifetime control in silicon. This diagram shows that VV(-/0), VP, V_2H, and V_2O(-/0) satisfy the condition Et-Ei < 0.2eV. For suppression of surge voltage, these traps are effective.

4. Conclusions

In summary, the effects on the surge voltage of trap energy levels resulting from localizing traps at the anode side were investigated in silicon power diodes. It was found that deep trap energy levels suppressed surge voltage at 1000A/cm^2 or less current density regions, and that shallow trap levels reduced surge voltage at over 1000A/cm^2.

References

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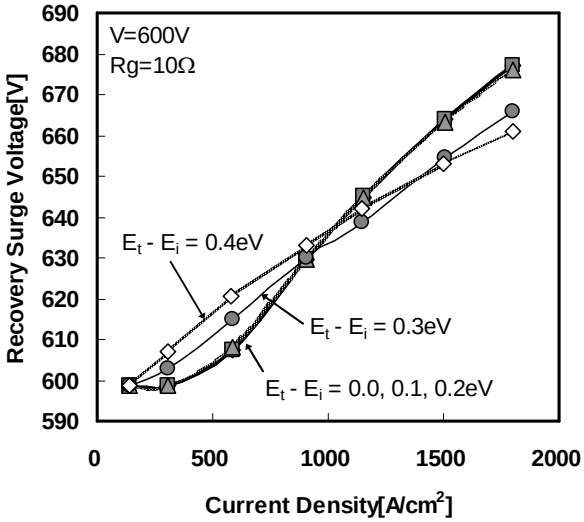

Fig. 4 Simulated dependence of recovery surge voltage with various trap energy levels (T=300K).

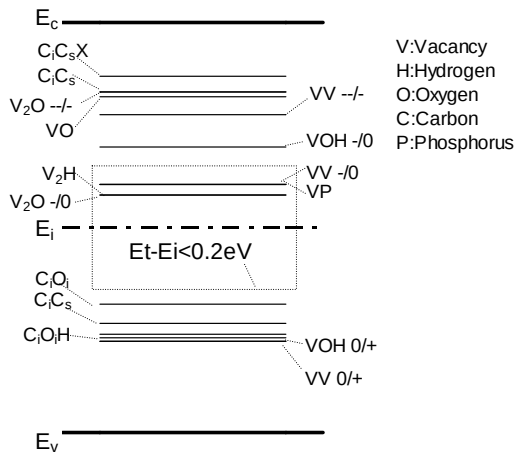

Fig. 5 Diagram of trap energy levels created by local lifetime control in silicon[1],[5-8]