Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp1054-1055

Research and Development on Ga_2O_3 Power Devices

Masataka Higashiwaki[1], Kohei Sasaki[2,1], Man Hoi Wong[1], Takafumi Kamimura[1], Daivasigamani Krishnamurthy[1], Akito Kuramata[2], Takekazu Masui[3], and Shigenobu Yamakoshi[2]

[1] National Institute of Information and Communications Technology (NICT)
4-2-1 Nukui-kitamachi, Koganei, Tokyo 184-8795, Japan
Phone: +81-42-327-6092 E-mail: mhigashi@nict.go.jp
[2] Tamura Corporation
2-3-1 Hirosedai, Sayama, Saitama 350-1328, Japan
[3] Koha Co. Ltd.
2-6-8 Kouyama, Nerima, Tokyo 176-0022, Japan

Abstract

We have been developing new widegap compound semiconductor gallium oxide (Ga_2O_3) transistors and diodes. Here, we will introduce current status and future prospects of research and development on Ga_2O_3 power devices.

1. Introduction

We have been proposing a new oxide compound semiconductor, gallium oxide (Ga_2O_3), as a promising candidate for power device applications because of its excellent material properties and suitability for mass production [1]. The 4.8-eV bandgap and the Baliga's figure of merit (FOM) of Ga_2O_3 are much larger than those of SiC and GaN, which will enable Ga_2O_3 power devices with higher breakdown voltage (V_{Br}) and efficiency than SiC and GaN devices. The other important advantage of Ga_2O_3 is that a single-crystal bulk can be grown by using the same melt growth method as is used for sapphire. Therefore, Ga_2O_3 power devices have the obvious potential to surpass SiC and GaN in not only device performance but also cost effectiveness.

In this abstract, we mainly describe most recent results on depletion-mode Ga_2O_3 metal-oxide-semiconductor field effect transistors (MOSFETs).

2. Appealing points of Ga_2O_3 for power device applications

Based on the material parameters, the Baliga's FOM of Ga_2O_3 is expected to be at least four times larger than those of GaN and SiC. The same parameters also predict that Ga_2O_3 power devices will exhibit a lower theoretical on-resistance limit than other mainstream power devices at a given V_{Br}, as shown in Fig. 1.

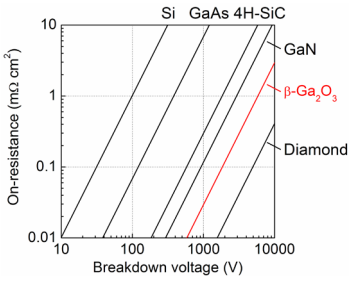
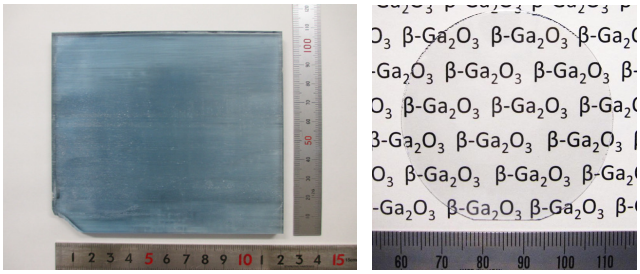


Fig. 1: Theoretical limits of on-resistances as a function of V_{Br}.

Another important advantage of Ga_2O_3 is that large-area single-crystal substrates can be fabricated from melt-grown bulk crystals. The edge-defined film-fed growth (EFG) method, which is one of the melt growth methods and has already been adopted to produce large sapphire wafers of over 8 inches in diameter, will be especially useful for low-cost mass production of Ga_2O_3 wafers since it does not require a high-temperature or high-pressure environment and uses less source material. Figures 2(a) and (b) show a 4-inch-square bulk β-Ga_2O_3 single-crystal plate grown by EFG and a 2-inch-diameter single-crystal Ga_2O_3 wafer, respectively. The crystal quality of the Ga_2O_3 wafer is very good, with a full width at half maximum of the x-ray rocking curve peak as narrow as 19 arcsec and a surface etch pit density on the order of 10^4 cm^{-2}.



(a) (b)

Fig. 2: Photographs of (a) a 4-inch-square bulk β-Ga_2O_3 single crystal grown by EFG and (b) a 2-inch-diameter single-crystal Ga_2O_3 wafer.

3. Depletion-mode Ga_2O_3 MOSFETs

Si-ion implantation doping

Recently, we developed Si-ion (Si^+) implantation technology for Ga_2O_3 to obtain a high electron density for fabricating low-contact-resistance ohmic electrodes [2]. Multiple Si^+ implantations were carried out at room temperature to form a 150-nm-deep box profile in unintentionally-doped Ga_2O_3 substrates. The total Si concentration was set at 1×10^{19}, 2×10^{19}, 5×10^{19}, or 1×10^{20} cm^{-3}. After the implantation, the samples were annealed for activation in a nitrogen gas atmosphere for 30 min by using an infrared-lamp annealing system. Figure 3 shows the annealing temperature (T_a) dependence of the effective carrier density (N_d-N_a) estimated by electrochemical capacitance-voltage measure-

ment. All samples show clear activation of the implanted Si atoms above T_a=800°C and sufficiently large N_d-N_a for the purpose of making ohmic contacts.

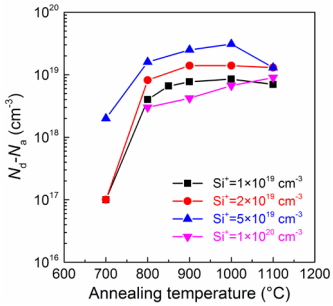
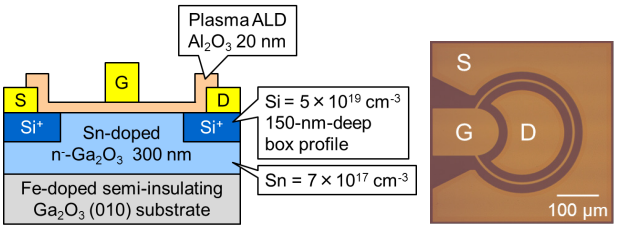


Fig. 3: T_a dependences of N_d-N_a in Si$^+$-implanted Ga_2O_3.

Depletion-mode Ga_2O_3 MOSFETs

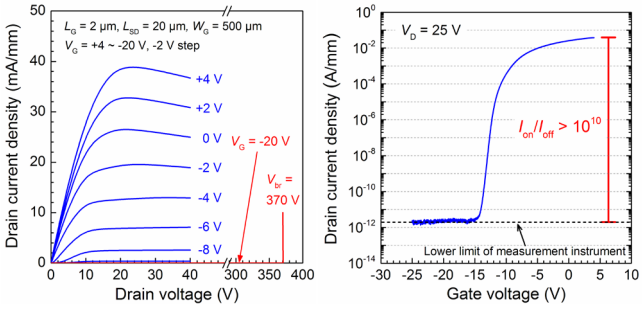
We fabricated depletion-mode Ga_2O_3 MOSFETs on Fe-doped semi-insulating single-crystal β-Ga_2O_3 (010) substrates. A Sn-doped *n*-Ga_2O_3 channel layer with a thickness of 300 nm was grown on the substrate by molecular-beam epitaxy [3]. Ga and Sn were supplied from conventional Knudsen cells. A gas mixture of ozone and oxygen was used as the O source. The Sn doping concentration was set at 7×10^{17} cm^{-3}. The activation energy of Sn in Ga_2O_3 was estimated to be about 60 meV from our previous work; therefore, about half of the Sn dopants were activated in the Ga_2O_3 epitaxial layer. Figures 4(a) and (b) show a schematic cross section and an optical micrograph of the Ga_2O_3 MOSFET, respectively. We employed a circular FET pattern as shown in Fig. 4(b). Multiple Si$^+$ implantations were performed to the regions for source and drain electrodes to form a 150-nm-deep box profile with Si=5×10^{19} cm^{-3}, followed by activation annealing at 925°C for 30 min. Then, a Ti/Au metal stack was deposited on the implanted regions and annealed again at 470°C for 1 min in a nitrogen gas atmosphere. We obtained a specific contact resistance as low as 8.1×10^{-6} Ωcm^2 for the annealed contacts. This is comparable to typical values for conventional Ti/Al-based alloyed contacts on *n*-GaN and/or AlGaN/GaN heterostructures. A 20-nm-thick Al_2O_3 gate dielectric and passivation film was formed on the Ga_2O_3 layer at 250°C by plasma atomic layer deposition. The gate metal was formed with Ti(3 nm)/Pt(12 nm)/Au(280 nm) on top of the Al_2O_3 film. The gate length and width were 2 and 500 µm, respectively. The spacing between the source and drain Si$^+$-implanted regions was 20 µm.

Figure 5(a) shows the DC output characteristics of the Ga_2O_3 MOSFET. The drain current (I_D) was effectively modulated by the gate voltage (V_G) with good saturation and sharp pinch-off characteristics. The maximum Id was 39 mA/mm at V_G=+4 V. The three-terminal off-state V_{Br} was as high as 370 V at V_G=-20 V. The transfer characteristic of the MOSFET at a drain voltage of 25 V is shown in Fig. 5(b). The I_D on/off ratio was extremely high, exceeding 10 orders of magnitude with the measured off-state leakage reaching the lower limit of the measurement instrument. These Ga_2O_3 MOSFET characteristics were much better than those of the Ga_2O_3 MESFETs we had reported previously [1]. We attribute the superior behavior of the MOSFETs to not only the large decrease in the contact resistance of the source and drain electrodes fabricated by using Si$^+$ implantation but also the low leakage current owing to the Al_2O_3 gate dielectric.



(a) (b)

Fig. 4: (a) Schematic cross section and (b) optical micrograph of Ga_2O_3 MOSFET.



(a) (b)

Fig. 5: (a) DC output and (b) transfer characteristics of Ga_2O_3 MOSFET.

4. Conclusions

We fabricated depletion-mode Ga_2O_3 MOSFETs on single-crystal β-Ga_2O_3 (010) substrates. All the device characteristics demonstrated the great potential of Ga_2O_3 electron devices and will pave the way for future high-power and high-voltage device applications.

Acknowledgements

This work was partially supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

References

[1] M. Higashiwaki et al., Appl. Phys. Lett. 100 (2012) 013504.

[2] K. Sasaki et al., submitted to Appl. Phys. Exp (2013).

[3] K. Sasaki et al., *Abstracts of the 40th International Symposium on Compound Semiconductors* (2013) 34.