

Gate Oxide Reliability on Large-Area Surface Defects in 4H-SiC Epitaxial Wafers

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Abstract

The reliability of gate oxide on large-area surface defects (trapezoid-shape and obtuse triangular defects) in 4H-SiC epitaxial wafers is discussed. Time-dependent dielectric breakdown measurements revealed that the decrease of charge-to-breakdown occurred at a MOS capacitor including the downstream line of those defects. Cross-sectional TEM image and the simulation of the electric field indicate that non-uniformity of oxide thickness causes the degradation of the reliability of the gate oxide.

1. Introduction

Improvements of the reliability of MOSFETs are crucial for the implementation of commercial SiC power device applications. Considering the oxide reliability of SiC MOSFETs, there are many studies being performed in order to clarify the influence of defects in SiC wafers on the gate oxide reliability [1-3].

It is well known that there are various surface defects such as “micro-pipe”, “down fall”, “carrot”, “comet”, “triangular defect” in SiC epitaxial wafers. Recently the density of those surface defects has been gradually decreasing with an improvement of the wafer quality. Large-area surface defects such as obtuse triangular defects [4], trapezoid-shape defects [5] have come to be relatively outstanding instead.

In this study, we utilize Time-Dependent Dielectric Breakdown (TDDB) measurements on SiC MOS capacitors to better understand the reliability of gate oxide on those large-area surface defects.

2. Experimental

N-type 4H-SiC(0001) epitaxial wafers with the off-cut angle at 4° toward [11-20] direction were used in this study. The effective carrier density and the thickness of the epitaxial layer were $1 \times 10^{16} \text{ cm}^{-3}$ and 10 μm , respectively. Confocal differential interference contrast (C-DIC) microscope (SICA by Lasertec Corporation) was used to detect surface defects on epitaxial layer.

We fabricated small area MOS capacitors with aluminum gate in the whole area of the wafer to assess impact on the reliability from surface defects. Gate oxide films were

thermally grown by dry oxidation at 1200 °C. After the dry oxidation, wafers were *in-situ* annealed in N₂ atmosphere for 30 min, resulting in an oxide thickness of about 42 nm. The capacitor is circle-shape of 140 μm in diameter.

TDDB measurements were performed at room temperature under the constant-current stress of 0.45 mA/cm² to examine the reliability of thermal oxides.

3. Results and Discussion

Figure 1 shows typical two types of large-area surface defects detected in C-DIC images. Trapezoid-shape defects* consist of upstream and downstream lines (Fig. 1(a)). These lines were normal to the off-cut and the step-flow directions. The lengths of upper and lower bases of the trapezoid were around 1mm and 10mm, respectively. We also observed obtuse triangular defects in the same sample (Fig. 1 (b)). The length of the base was at the same level as that of lower base of the trapezoid. The height of both defects (h) was around 140 μm , which corresponded to the distance calculated from epitaxial layer thickness d (10 μm) and 4 degree off axis angle ($h = d / \tan 4^\circ$). This suggests sources of both defects locate at or close the interface between epitaxial layer and substrate.

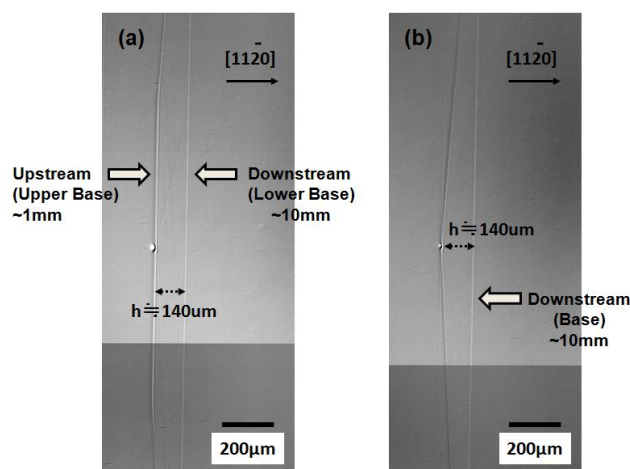


Fig. 1 C-DIC images of trapezoid-shape defect (a) and obtuse triangular defect (b).

*These defects are different type from the similar name defects “trapezoid defects” which consists of Frank type stacking-faults in epitaxial film [6].

In this study, the size of MOS capacitors is comparable to the “height” of the surface defects. We identified the relative position of MOS capacitor to the surface defects using C-DIC full wafer map after device process.

Fig. 2 indicates Weibull distribution plots measured from MOS capacitors including trapezoid-shape defects. Charge-to-breakdown (Q_{bd}) of MOS capacitors including lower base line of the trapezoid was approximately a half compared to those of MOS capacitors in the defect free area. On the contrary, in the case of the upper base or legs of the trapezoid, the decrease of Q_{bd} was very small. This result was also confirmed for the obtuse triangular defects. That is, Q_{bd} value of MOS capacitor including base line of the obtuse triangle was about a half compared to that of MOS capacitor in the defect free area.

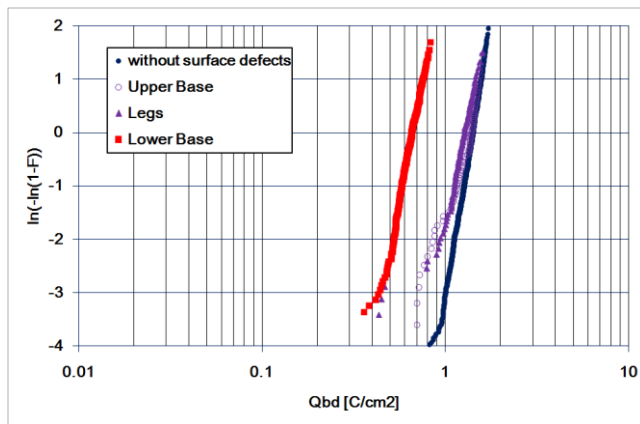


Fig. 2 Weibull distribution plots of MOS capacitor including Trapezoid-shape defect.

Cross-sectional TEM observation across the downstream line of trapezoid-shape defects was carried out to investigate the cause of decrease of Q_{bd} . As shown in Fig. 3, multiple bunched steps at the interface of SiO_2 /epitaxial layer and thickness fluctuation of oxide were observed. The maximum SiO_2 thickness (~ 55 nm) was located facing the multiple bunched steps, which is 30% thicker than the SiO_2 thickness on the terrace. The large oxide thickness fluctuation would lead to the local electric field concentration during TDDDB measurements [7].

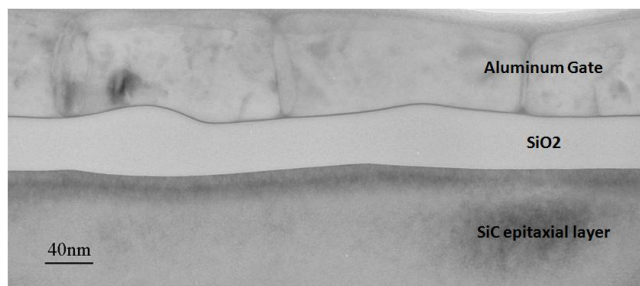


Fig. 3 Cross-sectional TEM image of SiO_2 /SiC structure across the downstream line.

The electric field in the gate oxide region was simulated using the configuration extracted from the TEM image. Fig. 4 expresses a simulation result when an applied voltage to aluminum gate was 42V that is the mean value dur-

ing the TDDDB measurements. The local electric field concentration is observed at the surface of oxide and the electric field in this area is approximately 20% stronger than that in the other area. It is thought that the density of Fowler-Nordheim tunneling current is higher in this region, thus resulting in a preferential breakdown of MOS capacitors including downstream lines.

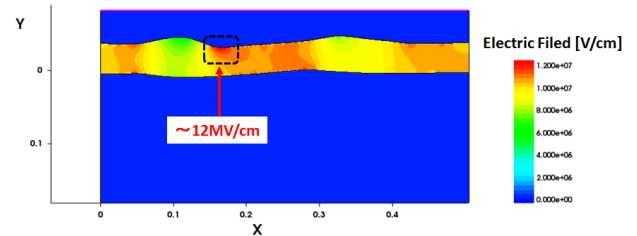


Fig. 4 Simulated electric field in the gate oxide region.

4. Conclusions

We investigated the reliability of gate oxide on large-area surface defects (trapezoid-shape, and obtuse triangular defects). Q_{bd} values of the MOS capacitor including downstream lines were about a half compared to those in defect free area. This degradation is caused by the electric field enhancement due to the non-uniformity of oxide thickness on a downstream line. Reduction of multiple bunched steps in the epitaxial wafer is important to improve the reliability of SiC MOS devices.

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