Strategy of STT-MRAM Cell Design and Its Power Gating Technique for Low-Voltage and Low-Power Cache Memories

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Abstract

Memory design methodologies for STT-MRAMs are presented. It is stressed that fine-grained power gating technique plays a key role in designing low-power and high-performance differential pair type STT-MRAMs. Comparison of memories using several differential pair type cells with SRAM is given. The 64B access in 32MB 4T2MTJ STT-MRAM consumes about 95% smaller write power than SRAM counterpart in 90nm technology node.

1. Introduction

Nonvolatile (NV) RAM using spin-transfer-torque magnetic tunnel junction (STT-MTJ) is regarded one of the key devices for realizing the future ultra-low-power computers [1]. A 1T1MTJ memory is intended to replace DRAM as NV main memory because of its smallest cell size. However, its access time is not fast enough to be used in embedded memories like cache [2]. For such applications, differential pair type cells will be suitable, because their access time can satisfy the specifications required by them.

However, since the MTJ-based differential pair type cells operate under power supply voltage, the power control in the cells is important for reducing their static power. This power gating technique is reviewed and we compare the power of STT-MRAMs using differential pair type cells in the power gating scheme with SRAM.

2. MTJ-based Differential Pair Type Memory Cells

Fig. 1 shows MTJ-based differential pair type memory cells [3-6]. They all have a structure in which a pair of MTJs are combined with positive feedback loops in MOSFET latches. Since power supply voltage ($V_{dd}$) and ground voltage (GND) are used for all cells, the subthreshold leak and the leak through MTJs (for Fig. 1 (b) and (d)) flow when they are powered. It is worth noting that all cells usually require two cycles in saving data to a pair of MTJs, though all but the 6T2MTJ cell in Fig. 1 (c) have possibilities to save data to MTJs in a single cycle.

3. Write Current Comparison

The write powers of the three cells in Fig. 1 (b), (c) and (d) are compared with 6TSRAM under the condition that they are power-gated in a row direction. We exclude the cell in Fig. 1 (a), because its operation doesn’t fit a fine-grained power gating scheme.

![Fig. 1 Differential pair type STT-MRAM cells](image)

![Fig. 2 Write cycles for the cells in Fig. 1 (b), (c), (d), and 6TSRAM cell to compare their powers](image)
width latch FETs and 0.4 µm width switch FETs. Under these conditions, we simulated the write cycles in 15ns in which 3ns period is assigned for the both MTJ switching periods (P to AP and AP to P). The power supply voltage of all the cells are denoted by PL and controlled as shown in Fig. 2 in the fine-grained power gating schemes. Fig. 3 shows the simulated currents that flow from each $V_{dd}$ to each cell. The $V_{dd}$ drives all controllers for the cells. The 4T2MTJ cell operates at the lowest $V_{dd}$ and is shown to consume the smallest current next to SRAM. Then we calculated each array current for 64B write in 32MB memory with L3 cache envisioned as shown in TABLE, where the array control currents stand for WL, BL, PL and SL charging currents assuming $C_{WL}=100fF$, $C_{PL}=C_{SL}=100fF$ (32b-grain) and $C_{WL}=1pF$. The subthreshold currents of NFET and PFET in the simulations are 6.8nA/µm and 3.4nA/µm, respectively, in 90nm technology node at 0.9V. The SRAM cell consumes 5.43nA static current. Therefore, the leak current of the 32MB SRAM is estimated 1458mA. The 32MB 4T2MTJ STT-MRAM can reduce the write current of 6TSRAM by 95% to 68mA in 90nm node.

4. Power Gating Techniques Applied to Memory

The power gating is a technique that cuts off $V_{dd}$-GND current paths of a circuit when it is not working [7]. The application of the technique to memories can be categorized into four methods as shown in Fig. 4. A group of cells that are gated by a power controller is often called a grain. The operation power, access time and write time can be reduced as the grain size decreases. Therefore, the 0D (pinpoint) power gating where every cell is gated by a power controller provides the best performance. However, the overhead of cell size is the maximum. Therefore, the 1D power gating brings about the optimum solution in the trade-off between the array size and the performance.

### TABLE

<table>
<thead>
<tr>
<th>Memory Cell</th>
<th>CMOS/MTJ Add-on Type</th>
<th>CMOS/MTJ Hybrid Type</th>
<th>NMOS/MTJ Hybrid Type</th>
<th>STT-MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ref}$</td>
<td>1.2V</td>
<td>1.9V</td>
<td>0.9V</td>
<td>0.9V</td>
</tr>
<tr>
<td>Total Current/32MB</td>
<td>133mA</td>
<td>217mA</td>
<td>68mA</td>
<td>1463mA</td>
</tr>
<tr>
<td>Components</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Write Current/64B (Write Current/cell)</td>
<td>120mA</td>
<td>196mA</td>
<td>62mA</td>
<td>1.4mA</td>
</tr>
<tr>
<td></td>
<td>234µA</td>
<td>382µA</td>
<td>120µA</td>
<td>3 µA</td>
</tr>
<tr>
<td>Static Current/32MB</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1458mA</td>
</tr>
</tbody>
</table>

Fig. 3 Currents flowing from each power supply voltage to each memory cell in the write simulations shown in Fig. 2.

Of the two 1D power gating methods in Fig. 4 (b) and (c), the row power gating in Fig. 4 (b) will be the preferable one. In almost memories, several cells along a WL are accessed in multi-bit organizations or in serial access modes. In such memory configurations, the row power gating scheme provides more efficient activation (wake-up) of cells than the column power gating one, when the accessed bits are assigned to the cells in the activated grain.

There have been proposed several row-directional power gating schemes in which PL driver design provides additional functions. The AND-type CMOS PL driver is suitable for 32b grain [8]. For smaller grain like 8b, a more compact NFET bootstrap PL driver was proposed [9]. A functional PL driver realizing a background write can be used for achieving an ultra-fast write cycle [4].

5. Conclusions

Power gating technique is indispensable for power reduction in the memories using the differential pair type STT-MRAM cells. The 1D row-directional fine-grained power gating is appropriate for the memory access modes. The 4T2MTJ cell consumes the smallest write power among the differential pair type cells, reducing 32MB L3 SRAM cache write power by about 95% in 90nm node. The STT-MRAM will become much more power-effective than SRAM by scaling both MOSFET and MTJ.

Acknowledgements

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References