A Normally Off Microcontroller Unit with an 84% Power Overhead Reduction Based On Crystalline In-Ga-Zn-Oxide Thin Film Transistors

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Abstract

A low-power normally off microcontroller unit (NMCU) having state-retention flip-flops using c-axis aligned crystalline In-Ga-Zn-oxide TFTs and employing a distributed backup and recovery method is fabricated. The NMCU employing a distributed backup and recovery method can reduce power overhead by about 84% and power consumption by about 22% compared to an NMCU employing a centralized backup and recovery method. Further, the NMCU can start main processing after a power on sequence about 74 μs earlier.

Introduction

These days, according to social needs for energy harvesting and sensor network system, a microcontroller unit (MCU) requires not only a reduction in dynamic power but also a reduction in static power. A power gating (PG) technology using a nonvolatile memory has attracted much attention in order to reduce static power [1]-[3]. When a conventional MCU uses a power gating (PG) technology, it is necessary to transfer data between nonvolatile memories and a CPU core, volatile registers, and local memories. We call this method a centralized backup and recovery method. The centralized backup and recovery method has problems of power overhead and time overhead, when the CPU core, the volatile registers, and the local memories store data in and recall data from the nonvolatile memories. To reduce power and time overheads in the centralized backup and recovery method, data is transferred between distributed nonvolatile memories and a CPU core, volatile registers, and local memories. The distributed nonvolatile memories are placed close to the CPU core, the volatile registers, and the local memories. We call this method a distributed backup and recovery method. In order to effectively use the PG technology, the MCU preferably employs a distributed backup and recovery method. There are many existing nonvolatile memories. A flash memory has low access speed and high power consumption, and a current-driven nonvolatile memory (e.g., a spin transfer torque magneto resistant RAM (STT-MRAM)) has high power consumption. The characteristics of these memories are insufficient to perform distributed backup and recovery.

We have discovered that a c-axis aligned crystalline In-Ga-Zn-oxide TFT (CAAC-IGZO-TFT) has very low off-state current [4]-[6]. Thus, we have applied this characteristic to a memory and a CPU in combination with a CMOS [5]-[8]. We consider that state-retention flip-flops (SRFFs) using CAAC-IGZO-TFTs are effective for a distributed backup and recovery method. To confirm the effectiveness, we have fabricated a normally off microcontroller unit (NMCU) having SRFFs using CAAC-IGZO-TFTs and employing a distributed backup and recovery method.

Microcontroller Outline

Fig. 1 is a block diagram of the NMCU, Fig. 2 shows a photograph of the NMCU, and Table I shows specifications of the NMCU. The fabricated NMCU has an 8-bit CPU, a power management unit (PMU), analog/digital peripheral circuits, a clock generator, and a memory. A nonvolatile oxide semiconductor RAM (NOSRAM) [8] is used as the memory. The NMCU has SRFFs in the CPU and the peripheral circuits. The SRFFs are capable of holding data during power off. The PMU controls backup processing and recovery processing of the SRFFs. An 8-MHz clock and a 32-KHz clock are produced by a ring oscillator (RO) and a crystal oscillator (XTAL), respectively. The NMCU supports an active mode and a shutdown mode. Power consumption in an active mode is 148 μA/MHz at 8 MHz and 2.0 V. In a shutdown mode, units excluding the PMU are powered off. The NMCU fabricated with a 0.35-μm CMOS process technology and a 0.8-μm CAAC-IGZO-TFTs process technology.

SRFF Operation

Fig. 3 is a circuit diagram of the SRFF, and Fig. 4 is a timing chart of the SRFF. Each SRFF consists of a flip-flop part having standard flip-flops and an IGZO part retaining data. The IGZO part includes a CAAC-IGZO-TFT and a storage capacitor. A WE2 signal and an RE signal are set to a HIGH level and a LOW level, respectively, when the NMCU is in the active mode. Then, the IGZO part does not operate, and the flip-flop part indicates performance equivalent to that of the standard flip-flop. Data in the flip-flop part is backed up to the IGZO part by discharge and charge of the storage capacitor.

Measurements

In the measurements, using an evaluation program, power consumption in the distributed backup and recovery method is compared to power consumption in the centralized backup and recovery method. Fig. 5 shows sequences of the evaluation program. In the evaluation program, at 8 MHz, the lengths of frame periods are the same (1000 μs), and a main processing period is 514 μs. Main processings are output processing of a general purpose input/output (GPIO) and increment processing of internal registers. Fig. 6 shows
power consumption and its approximate straight line (dotted line). The power consumption is measured at the time of changing the number of increment processings to change the main processing period. The intercept of the approximate straight line corresponds to power overhead. Fig. 6 shows that power overhead in the distributed backup and recovery method can be reduced by about 84% compared to the centralized backup and recovery method. By comparing power consumptions in both the methods in Fig. 6, the use of the distributed backup and recovery method leads to a reduction in power consumption of the NMCU by about 22%. The measured power consumption in the centralized backup and recovery method does not include power consumption of a nonvolatile memory for data storage.

Next, Fig. 7 shows measurement results of sequences before the start of main processing in both the methods. The distributed backup and recovery method has an advantage that, at 8 MHz, main processing after the power on sequence can be started about 74 μs earlier than the centralized backup and recovery method.

We fabricate a NMCU having SRFFs using CAAC-IGZO-TFTs and employing a distributed backup and recovery method. The use of the NMCU leads to a reduction in power overhead by about 84% and a reduction in power consumption by about 22% compared to an NMCU employing a centralized backup and recovery method. Further, the NMCU can omit data storage processing after a power on sequence. Consequently, the NMCU can start main processing about 74 μs earlier. These results indicate that CAAC-IGZO-TFTs are effective in reducing power consumption and increasing access speed of an MCU.

**Conclusion**

We fabricate a NMCU having SRFFs using CAAC-IGZO-TFTs and employing a distributed backup and recovery method.

**Table 1 NMCU specifications.**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
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<tr>
<td>Architecture</td>
<td>8bit CISC</td>
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<tr>
<td>Technology</td>
<td>CMOS:0.35μm, CAAC-IGZO-FET: 0.8μm</td>
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<tr>
<td>Die size</td>
<td>11.0mm x 12.0mm</td>
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<tr>
<td>SRFF count</td>
<td>279</td>
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<tr>
<td>Clock frequency</td>
<td>8MHz</td>
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<td>Power supply voltage</td>
<td>2V</td>
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**References**