

# Studies on Selective Devices for Spin-Transfer-Torque Magnetic Tunnel Junctions

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## 1. Introduction

When MTJs are implemented into LSIs as nonvolatile memory devices, it is indispensable that they are designed so that they are to be selected by semiconductor devices such as MOSFETs, bipolar transistors or diodes. As for MOSFET selective devices, NFET, PFET [1] and CMOS devices have been used.

However, NFET and PFET devices cannot apply sufficient voltages between the two terminals of MTJs during MTJ switching for specific polarities of applied voltage, because they operate in saturation region for the directions. Though CMOS device can avoid the problem, its area is large due to well-substrate separation with well biasing and it needs two complementary control signals.

In this paper, we propose a new selective device for MTJs consisting of two NFETs, one working for selecting an MTJ and the other for boosting the gate voltage of the selective NFET. We compare the areas of the four devices (one proposed and three conventional devices) under an equal switching time constraint to figure out the smallest device. A scaling trend is also studied.

## 2. Boosted NFET Switching Device

Fig. 1 compares the structure of an MTJ connected in series with the boosted NFET selective device (d) with the three conventional selective device structures (a) NFET, (b) PFET [1] and (c) CMOS. It consists of two NFETs. One selects the MTJ, while the other works as a barrier transistor to boost the voltage of the selective NFET's gate (E) beyond the power supply voltage  $V_{dd}$  when the drain (Z) is set high prior to the rising of the drain voltage of the selective NFET (Y). This boosting makes the selective NFET operate in linear region when Y is set high with X low to effectively apply the switching voltage between the two terminals of the MTJ in both directions.

Fig. 2 (a) shows the variation in the voltage of internal nodes (D, E) along with the external nodes (Y, Z).  $V(E)-V(D)$  and  $V(E)-V(Y)$  are shown not to exceed  $V_{dd}$  as shown in Fig. 2 (a). Therefore, there is no concern about the gate oxide reliability by this gate voltage self-boosting. On the other hand, it is worth noting that  $V_{gs}$  exceeds  $V_{dd}$  when the selective signal itself (Z) is boosted with the drain (Y) remained low in the conventional NFET structure Fig. 1 (a).

## 3. Device Area Comparison

Fig. 3 shows the switching characteristics of a 100nm $\phi$  perpendicular MTJ (p-MTJ) that is modeled in SPICE simulations we performed in this paper [2]. By using this built-in MTJ model, we can simulate MTJ/CMOS hybrid circuits accurately.

Fig. 4 shows the switching characteristics of the four structures in 90nm CMOS and 100nm $\phi$  MTJ technologies at  $V_{dd}=1.0V$  when Y is raised high with X low to switch MTJs from parallel (P) to anti-parallel (AP) in the case of

bottom-pin as shown in Fig.1. The channel length is  $L_g=0.1\mu m$  for both NFET and PFET and the channel widths of the selective devices are (a)  $W_n=4\mu m$ , (b)  $W_p=2.4\mu m$ , (c)  $W_n=1.4\mu m$ ,  $W_p=0.7\mu m$  and (d)  $W_{n-select}=0.85\mu m$ ,  $W_{n-barrier}=0.2\mu m$ . By choosing these channel widths, all structures switch the MTJ from P to AP within 10ns as shown in Fig. 4. The opposite (AP to P) switching times are also shown to be within 10ns in Fig. 5.

We optimized the total channel widths (a)  $W_n$ , (b)  $W_p$ , (c)  $W_n+W_p$ , (d)  $W_{n-select}+W_{n-barrier}$  for the four structures by changing  $V_{dd}$  from 0.8V to 1.2V (optimized separately for each  $V_{dd}$ ) as shown in Fig. 6. As shown in Fig. 7 and Fig. 8, the switching speeds for all cases are within 10ns. To transform the total channel widths into corresponding physical layout areas, we drew the four structures optimized for  $V_{dd}=1.0V$  by using 90nm design rules as shown in Fig. 9. The areas of the structures are easily estimated from Fig. 6 and the layouts 6, as shown in Fig. 10. The results show that the boosted NFET structure brings about the smallest selective devices for the 90nm CMOS and 100nm $\phi$  MTJ technologies at  $V_{dd}=1.05V$  and below.

## 4. Scaling Trend

The scaling of the four structures from 90nm to 32nm is studied. MOSFETs and MTJs are assumed to be scaled as shown in Table. Fig. 11 shows the scaling trend of the areas of the four selective devices. Fig. 12 shows the switching speeds for the devices in Fig. 11. It is worth noting that NFET's scaling stops and that even PFET's scaling saturates both at 32nm. On the other hand, the boosted NFET and CMOS scale well. Though the boosted NFET is the smallest at 32nm or larger, CMOS is also an attractive choice for the smaller generations.

## 5. Conclusions

We proposed a novel structure that selects an MTJ by a self-boosted NFET. It was found that the structure realizes smaller selector for MTJs compared with the conventional ones under the same switching time constraint. It was also predicted that the proposed selector together with the CMOS structure remains scalable, while NFET and PFET stop scaling at 32nm and beyond. This technology can be applied to any MTJ/CMOS hybrid circuit such as NV-FPGA's crossbar switch [3], NV-latch circuit [4] and so on (see Fig. 13). It is also useful for slower applications such as NVMs: e.g. 1T1MTJ cell and 4T2MTJ cell [5].

## Acknowledgements

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## References

- [1] H. Koike and T. Endoh, *SSDM*, pp. 961-962, 2011. [2] N. Sakimura et al., *ISCAS*, pp. 1971-1974, 2012. [3] T. Endoh et al., *Japanese Patent Application* 2012-3. [4] Endoh et al., *IEDM*, pp. 75-78, 2011. [5] T. Ohsawa et al., *SSDM*, pp. 959-960, 2011.

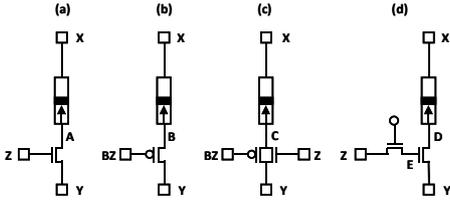


Fig. 1 Schematics of selective devices with MTJs: (a) NFET, (b) PFET, (c) CMOS, (d) boosted NFET (proposed).

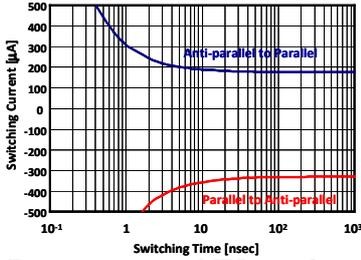


Fig. 3 100nmφ p-MTJ switching characteristics modeled in SPICE.

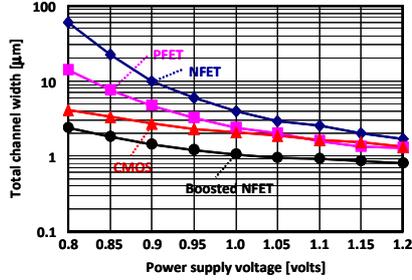


Fig. 6 Total channel widths of the selective devices as a function of  $V_{dd}$  in 90nm.

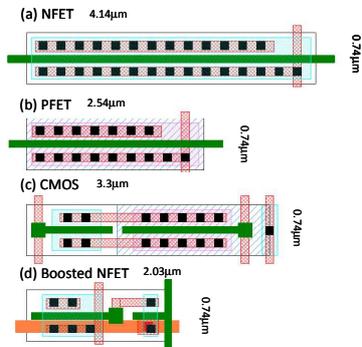


Fig. 9 Layouts of the selective devices in 90nm optimized for  $V_{dd}=1.0V$ .

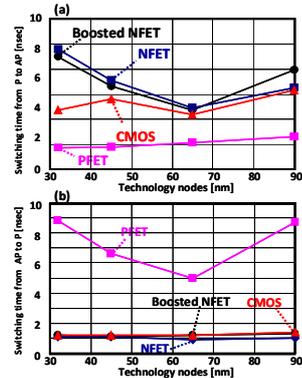


Fig. 12 Scaling trends of switching speeds: (a) P to AP, (b) AP to P.

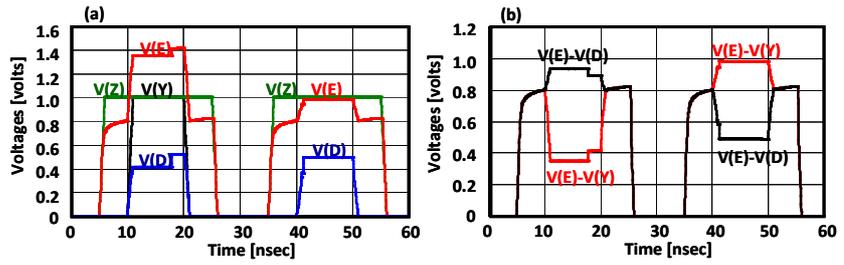


Fig. 2 (a) Voltage variation for internal nodes of proposed boosted NFET selective device, (b) Its gate-source/drain voltages.

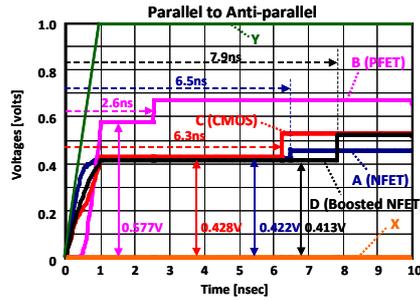


Fig. 4 P to AP switching at  $V_{dd}=1.0V$  in 90nm.

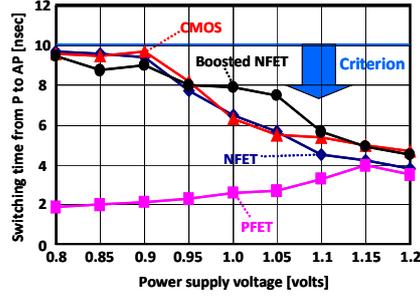


Fig. 7 P to AP switching times as a function of  $V_{dd}$  in 90nm node.

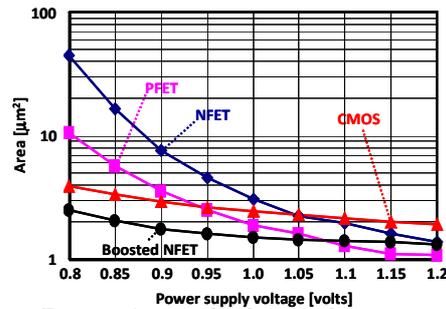


Fig. 10 Areas of selective devices as a function of  $V_{dd}$  in 90nm.

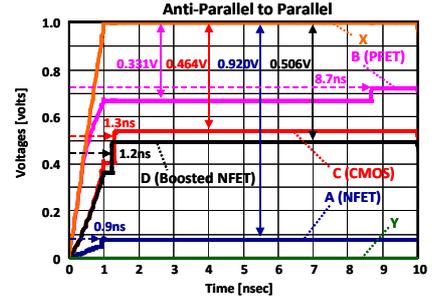


Fig. 5 AP to P switching at  $V_{dd}=1.0V$  in 90nm.

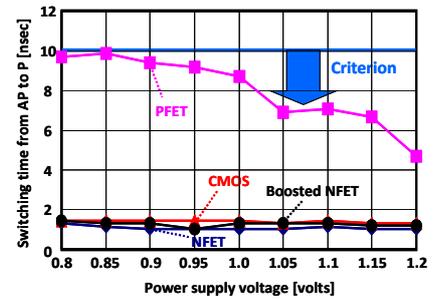


Fig. 8 AP to P switching times as a function of  $V_{dd}$  in 90nm node.

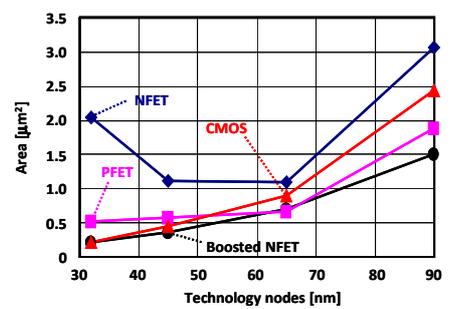


Fig. 11 Scaling trend of areas of the selective devices.

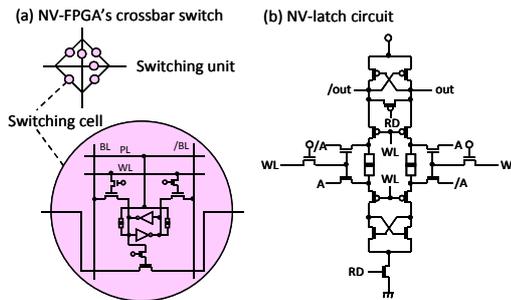


Fig. 13 Application examples of proposed boosted NFET selective device: (a) NV-FPGA's crossbar switch, (b) NV-latch circuit.

TABLE

MTJ and MOSFET PARAMETERS USED IN THE SCALING SIMULATIONS

Technology node [nm]	90	65	45	32
MTJ size [nmφ]	100	70	50	35
$R_p$ [kΩ]	1.2	2.4	4.8	9.6
$R_{ap}$ [kΩ]	2.56	5.12	10.24	20.48
$I_c$ (AP→P) [μA]	175	87	44	22
$I_c$ (P→AP) [μA]	330	165	83	42
$V_{dd}$ [V]	1	1	0.9	0.8
$L_g$ [nm]	100	70	50	35