Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp1190-1191

An Alternative Technique for GeOI Fabrication

Cheng-Ting Chung[1], Guang-Li Luo[2] Che-Wei Chen[1] and Chao-Hsin Chien[1,2]

[1] Department of Electronics Engineering & Institute of Electronics, National Chiao-Tung University,
No.1001, Daxue Road, East Dist., Hsinchu City 300, Taiwan, R.O.C.
[2] National Nano Device Laboratories,
No. 26, Prosperity Road 1, Science-based Industrial Park, Hsinchu City 30078, Taiwan, R.O.C.
Tel: +886-3-5726100 ext 7660, E-mail: *glluo@ndl.narl.org.tw*

Abstract

A kind of GeOI-like wafer is demonstrated by epitaxial growth of Ge on an unltra-thin SOI substrate. Employing high temperature annealing for 2 hrs in high vacuum ambient, the ultra-thin Si layer inter-diffuses with the grown Ge layer, and finally a uniform GeOI-like structure is formed. This structure can be easily applied to fabrication of Ge FinFET, Ge nanowire FET and even Ge junctionless FET devices.

1. Introduction

Germanium has been considered a promising material to replace silicon channel because of its higher carrier mobilities. However, smaller bandgap and higher permittivity of Ge causes severe reverse junction leakage current and short channel effects (SCEs). In recent years, silicon-on-insulator (SOI) structure has been widely investigated due to better electrostatic integrity. Therefore, germanium on insulator (GeOI) is a solution with the same concept of SOI to suppress junction leakage and SCEs. GeOI wafers have been demonstrated by many fabrication methods, including Ge condensation [1], smart-cut [2], and rapid melt growth (RMG) [3].

In this work, we demonstrate an alternative simple technique to perform high quality GeOI wafers. Based on the epitaxial Ge on ultra-thin body SOI substrate accompanying with high temperature annealing, much GeOI-like wafers can be obtained.

2. Experimental

Fig. 1 shows the process flow of the epitaxial GeOI wafer. 6-inch (100) SOI wafers with 30 nm Si device layer were used in this experiment. Firstly, the Si device layer was oxidized in O_2 ambient. Then, the oxide was carefully removed by chemical wet etching, and the Si device layer could be thinned down to 5 nm by these procedures. After standard cleaning, the substrates were dipped in dilute HF and immediately introduced to ultra-high vacuum chemical vapor deposition (UHVCVD) chamber. The base pressure of the UHVCVD chamber was $\sim 5\times10^{-9}$ torr. First step of the deposition process was baking wafer at 900 ℃ for 10 min in high vacuum ambient to ensure that the wafer surface was clean, and 125-nm Ge layer was grown at 420 ℃ with germane (GeH_4) precursor. The deposition condition could avoid island growth. *In-situ* high temperature annealing was performed at 900 ℃ with 1 – 2 hrs to investigate the intermixing effect of Si/Ge.

4. Results and Discussion

Fig.2 shows the cross-sectional TEM image of the 1-hr annealed sample. After 900 ℃ annealing for 1 hr, the Si layer still exists under the epitaxial Ge film. However, the interface of Si/Ge becomes rough, indicating intermixing of Si/Ge occurs during high thermal budget annealing. Besides, dislocations can be observed in Ge film due to the large lattice mismatch between Si and Ge (4.2%). In order to reduce the interface roughness and improve film quality, 2-hrs annealing is carried out to increase the thermal budget, as shown in fig. 3. From the TEM images, the ultra-thin Si layer disappears after Si/Ge intermixing, and a uniform high Ge content layer is formed on the buried oxide. Because the original Si layer is ultra-thin, the Si content in the newly formed layer is very low. This structure is much like a GeOI structure. Moreover, dislocation density is obviously decreased after annealing.

In order to briefly analyze the distribution of Si atoms in Ge film, SIMS result of 900 ℃ 2-hrs annealed sample is shown in fig. 4. Si atoms diffuse into Ge film uniformly, and the Si concentration is around 10^{21} ~ 2×10^{21} atom/cm^{-3}. We can estimate the percentage of Si from the SIMS concentration, and the Si content is about 2.21%. High Ge-content (97.79%) GeOI substrate can be realized by this technique.

XRD analysis results are shown in fig. 5. The XRD peak of as-deposited sample is at ~66.3°, which is close to Ge bulk (004) peak position (~66°). After 1-hr annealed, two peaks can be observed at ~66° and ~66.5°, which possibly represent relaxed Ge and tensile strained Ge, respectively. It has been reported that the difference in thermal expansion coefficient between Si and Ge will cause tensile strain in Ge film during the cooling procedure [4]. In our case, for the uniform Si/Ge intermixing (2-hrs annealed) sample, the peak shifts toward higher 2θ angle, indicating that Ge layer also possesses a tensile strain. The full-width at half-maximum (FWHM) value of the 2-hr annealed sample is 0.188 degree, which is lower than the as-deposited (0.265 degree) and 1-hr annealed (0.201 degree) sample. It reveals that Ge film quality does be improved by high temperature annealing.

The root mean square roughness is measured by AFM as shown in fig. 6. Surface roughness is slightly increased after the high temperature annealing, and we speculate that intermixing effect may degrade roughness. However, 2-hr annealed sample exhibits better roughness, indicating that the surface will become smooth after Si/Ge intermixing. The mechanism behind this phenomenon needs to be further clarified.

3. Conclusions

In summary, by direct epitaxial growth of Ge layer on an ultra-thin SOI substrate and following high temperature post deposition annealing, a GeOI-like structure is formed. From SIMS and XRD results, the newly formed GeOI-like structure is a uniform layer. The Si content is only 2.21%, and the GeOI-like layer possesses a tensile strain. The high quality GeOI-like wafer demonstrated in this work can potentially provide a practical platform for Ge CMOS application.

References

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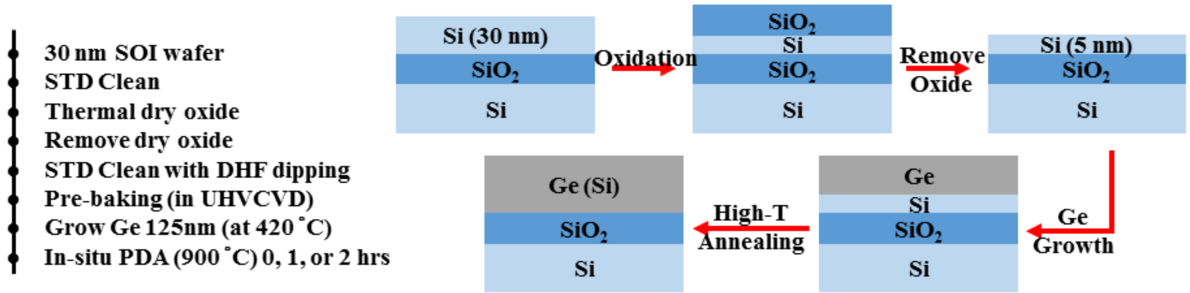

Fig. 1. Process flow for the formation of GeOI-like wafers. *In-situ* high temperature annealing is performed at 900 ℃ with 1 – 2 hrs to investigate the intermixing effect of Si/Ge.

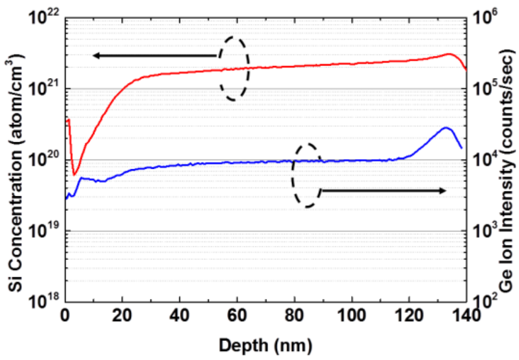

Fig. 4. SIMS profile of the 2-hrs annealed sample. The Si content is about 2.21% from the estimation of SIMS concentration.

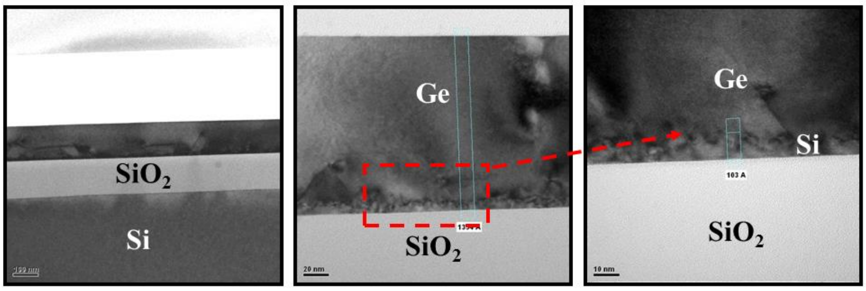

Fig. 2. Cross-sectional TEM image of the 1-hr annealed sample. The Si layer still exists under the epitaxial Ge film.

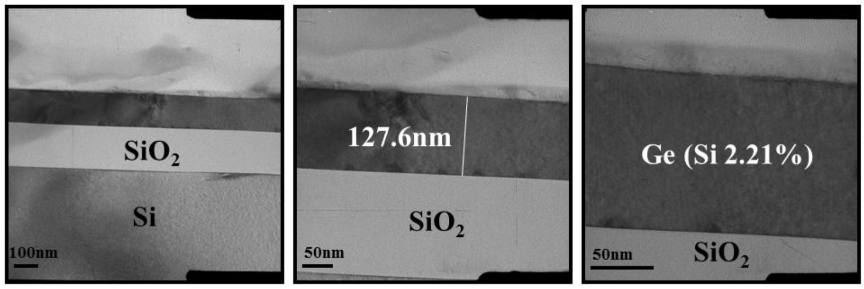

Fig. 3. Cross-sectional TEM image of the 2-hrs annealed sample. Ultra-thin Si layer disappears after Si/Ge intermixing.

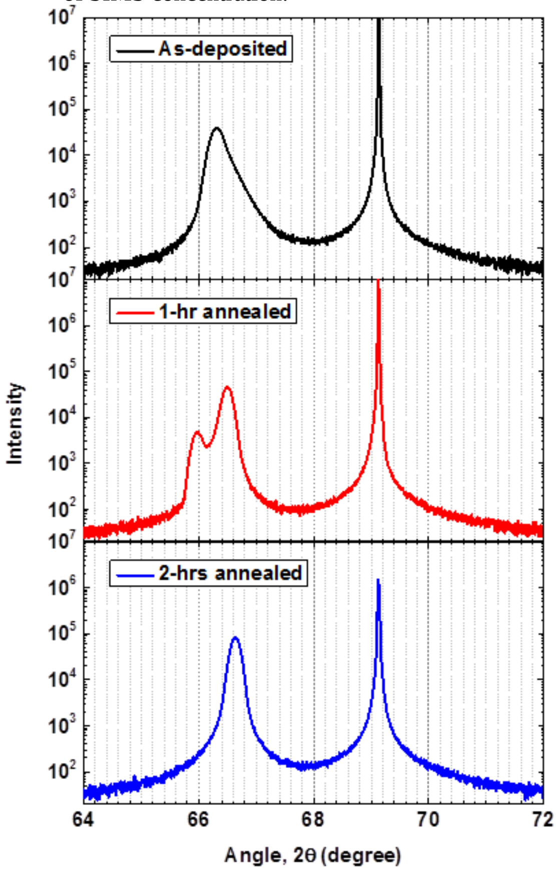

Fig. 5. XRD analysis of epitaxial Ge on ultra-thin SOI with different annealing condition.

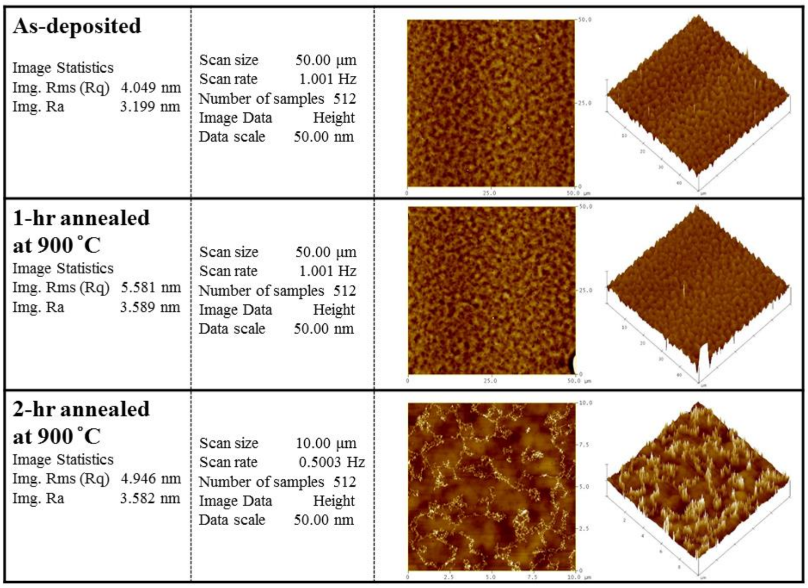

Fig. 6. Surface roughness of epitaxial GeOI substrates measured by AFM. Surface roughness is slightly increased after the high temperature annealing.