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Tensile strained GeSn on Si by solid phase epitaxy and fabrication of high mobility FET devices

Ruben R. Lieten[1,2], Tatsuro Maeda[3], Wipakorn Jevasuwan[3], Hiroyuki Hattori[3], Noriyuki Uchida[3], Shu Miura[4], Masatoshi Tanaka[4], Jin Won Seo[1], Jean-Pierre Locquet[1]

[1] KU Leuven, 3001 Leuven, Belgium
Phone: +32-16-32-7228 E-mail: ruben.lieten@fys.kuleuven.be
[2] IMEC, 3001 Leuven, Belgium
[3] National Institute for Advanced Industrial Science and Technology (AIST)
Tsukuba, Ibaraki 305-8562, Japan
[4] Yokohama National University
Yokohama, Kanagawa , 240-8501, Japan

Abstract

We demonstrate single crystalline $Ge_{1-x}Sn_x$ (GeSn) on Si by solid phase epitaxy (SPE) and subsequent fabrication of metal-oxide-semiconductor field-effect transistor (MOSFET) devices. Amorphous GeSn layers are obtained by limiting the adatom surface mobility during deposition. Subsequent annealing transforms the amorphous layer into single crystalline GeSn by solid phase epitaxy. Single crystalline GeSn layers with 4.5% Sn and +0.34% tensile strain are fabricated on Si(111) substrates. Additionally, we show depletion-mode operation of GeSn pMOSFETs on Si(111) using SPE, TaN/Al_2O_3 metal-gate/high-k gate stacks, and self-aligned Ni-based metal S/D contacts. We present good transfer characteristics with on/off ratio of 84 thanks to ultrathin GeSn layer on Si.

1. Introduction

GeSn has been predicted to exhibit carrier mobilities exceeding both that of Ge and Si, which makes GeSn suitable as alternative channel material in high-speed Si-CMOS technology. In addition, GeSn exhibits a direct band gap for Sn concentration of ±8%, and is therefore promising for optical applications [1]. While previous GeSn channel transistors were predominately fabricated on Ge substrates [1, 2], integration into Si is preferred for CMOS compatibility. Epitaxial growth of GeSn on Si substrates poses several challenges: the limited solubility of Sn in Ge (0.5%), compositional fluctuations, Sn segregation and large lattice mismatch (>4%). It is critical to suppress these effects for obtaining high performance devices with GeSn layers.

Recently, we demonstrated single crystalline GeSn layers on Si(111) substrates by solid phase epitaxy (SPE) of amorphous GeSn layers with excellent structural quality [3]. This technique is advantageous for the realization of ultrathin GeSn layers directly on Si, which have high potential for depletion-mode pMOSFET devices owing to the decent valence band offset between Si and GeSn. As bulk transport is dominant in depletion-mode devices [4,5], excellent GeSn bulk mobility can be fully utilized. In addition, our method leads to tensile strain in the GeSn layer, which enhances the carrier mobility further.

In this work, employing ultrathin single crystalline GeSn layer directly on Si substrates, we fabricate depletion-mode GeSn pMOSFETs with TaN/Al_2O_3 gate stack and NiGeSn metal S/D. We observe well-behaved junctionless GeSn pMOSFET operation thanks to ultrathin (<10 nm) GeSn channel layer.

2. GeSn on Si by SPE

40 nm amorphous GeSn (4.5% Sn) is deposited on insulating Si substrates with (111) orientation at RT. We limit the adatom surface mobility during deposition with the introduction of inert gas species to improve the quality of SPE [3]. Subsequent annealing at 600 ˚C for 1 minute transforms the amorphous GeSn into a single crystalline layer by SPE. An intense and narrow GeSn (331) diffraction peak is observed in a reciprocal space map (RSM) XRD scan, see Fig. 1, indicating high crystal quality. The (111) crystal planes of the GeSn layer are parallel to the (111) Si surface. From Hall effect measurement, the fabricated GeSn layer with a thickness of 40 nm shows a hole concentration of 1.6 x 10^{18} cm^{-3} corresponding to the Ga dopant concentration and hole mobility of 128 cm^2/Vs, which is higher than that of bulk Si (80 cm^2/Vs).

3. Device fabrication

Prior to the device fabrication, we reduced the GeSn layer thickness using RIE etching for 2 ~ 4 sec in order to turn off the depletion-mode devices. Then, we fabricated GeSn pMOSFETs with ALD Al_2O_3 dielectrics and self-aligned NiGeSn S/D. After surface cleaning, a 100-cycle Al_2O_3 layer was deposited as a gate insulator by ALD and PDA carried out at 400ºC. Next, a TaN metal gate was formed by sputtering and dry etching. Subsequently, 25 nm-thick Ni was deposited on the GeSn layer in order to form the NiGeSn metal S/D. Self-aligned Ni-based metal S/D for GeSn was fabricated by annealing at 350ºC for 1 min, followed by selective wet etching using a HCl solution to remove the unreacted Ni.

4. Electrical properties

Id–Vg characteristics of GeSn p-MOSFETs with <10 nm GeSn thickness (4 sec RIE etching) at Vd of -50mV and -1V is shown in Fig. 2. The device shows good transfer characteristics. We can successfully control Id with an On/Off ratio of 84 by reducing the GeSn thickness to thinner than its maximum depletion layer width. Fig. 3 shows the Id–Vd characteristics of a <10 nm-thick GeSn pMOSFET on Si with the gate length of 10 μm. These results indicate the first successful operation of depletion-mode junctionless GeSn pMOSFET on Si, employed by the SPE method. By decreasing the channel thickness from 40 nm to less than 10 nm, On/Off ratio is improved by more than one order of magnitude. While reducing the GeSn layer thickness increases the gate control of the channel, we observe hole mobility degradation (Fig. 4). This hole mobility reduction is attributed to the effects of severe surface roughening by RIE etching as well as the carrier scattering centers at the GeSn/Si heterointerface.

5. Conclusions

We have demonstrated depletion-mode operation of GeSn pMOSFETs on Si(111) using SPE of amorphous GeSn layers, TaN/Al_2O_3 metal-gate/high-k gate stacks, and Ni-based metal S/D contacts. We present good transfer characteristics with On/Off ratio of 84 owning to ultrathin (<10 nm) GeSn layer on Si. Further improvements in depletion-mode junction-less GeSn pMOSFETs can be obtained by controlling the structural properties of the GeSn layers on Si.

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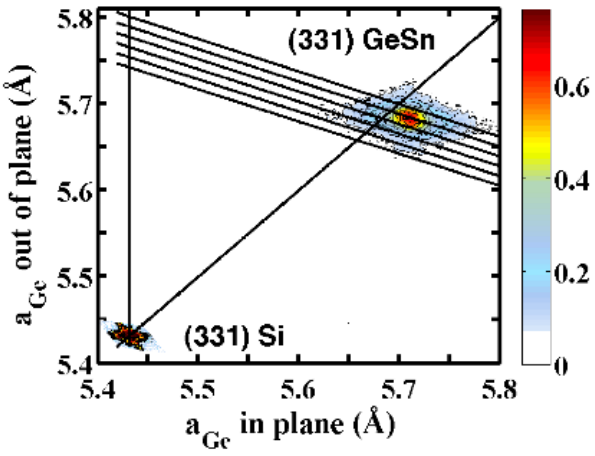

Fig. 1 XRD reciprocal space map around the (331) reflection of 37 nm crystallized GeSn (sample C, 4.5% Sn/(Sn+Ge) flux ratio), transformed to in-plane and out-of-plane lattice spacings. The color bar indicates the XRD intensity (arbitrary units) in log scale.

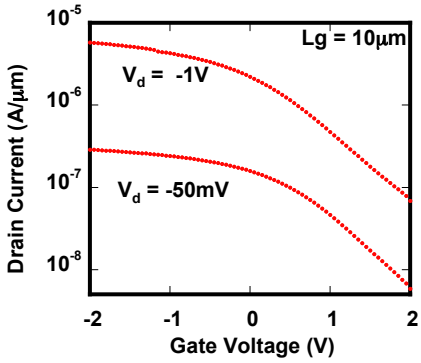

Fig. 2. Id-Vg characteristics of depletion-mode GeSn pMOSFETs with L = 10 μm and drain voltage of -50 mV and -1V. The On/Off current ratio of 84 is obtained between Vg = -2 and 2V at Vd = -1V.

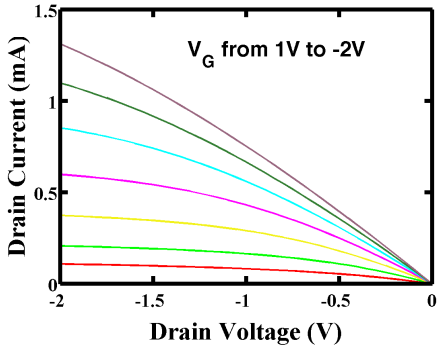

Fig. 3. Id-Vd characteristics of depletion-mode GeSn pMOSFETs with GeSn channel thickness of <10 nm for different gate voltages, showing clear channel control.

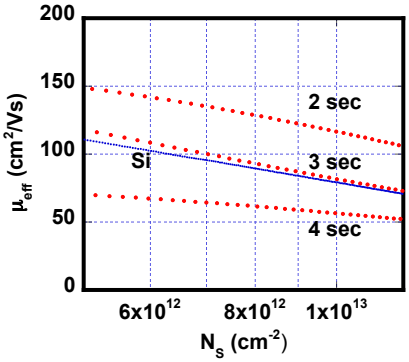

Fig. 4. Channel mobility of depletion-mode GeSn pMOSFETs for 2, 3, and 4 sec RIE channel thinned samples.

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