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Low-Temperature (~300°C) Epitaxial-Growth of SiGe(Sn) on Si-Platform by Liquid-Solid Coexisting Annealing

H. Chikita, R. Matsumura, Y. Tojo, Y. Kinoshita, T. Sadoh, and M. Miyao

Department of Electronics, Kyushu University, 744 Motooka, Fukuoka 819-0395, Japan

Tel : +81-92-802-3736 , FAX : +81-92-802-3724, E-mail : h_chikita@nano.ed.kyushu-u.ac.jp

Abstract

To develop a new low-temperature crystallization technique, annealing characteristics of a-GeSn/c-Si structures are examined as a function annealing temperature (200-1000°C) and Sn concentration (10-30%). By Sn-doping (~26%) into a-Ge, SiGe-mixing and epitaxial-growth temperatures are significantly decreased, which enables SiGe(Sn) epitaxial-growth at 300°C. These phenomena are attributed to liquid-phase-growth through partial-melting-channel running across liquid-solid coexisting region. This technique facilitates integration of multi-functional devices on Si-platform.

1. Introduction

Formation of high-quality Ge and SiGe layers on Si-platform is essential to realize next-generation LSIs. This is because Ge and SiGe have high carrier mobility compared with Si. In addition, they are ideal buffer layers for epitaxial growth of various optical- and spintronic-materials with different lattice constants. In line with this, we have developed SiGe mixing-triggered rapid-melting growth (process temperature: ~1000°C) [1,2] and realized defect-free single-crystal Ge and SiGe on Si platform [1-4]. To expand the application fields of this technique into 3-dimensional LSIs and thin-film transistors, decrease of growth temperatures down to ≤300°C is essential.

Recently, Nakatsuka et al. reported low-temperature (~400°C) formation of SiGe(Sn) by annealing of a-GeSn/Si stacked structures, which was attributed to solid-phase atomic mixing [5]. It is noted that the liquid-solid coexisting (L+S) region exists in the phase diagram of GeSn, as shown in Fig.1(a). Since the solidification point of GeSn is 231°C, we can expect that low-temperature (<300°C) liquid-phase growth should propagate through partially-melted channel running across the liquid-solid coexisting region. To realize such expectation, detailed annealing characteristics in the liquid-solid coexisting region should be clarified.

In the present work, we investigate growth characteristics of a-GeSn/c-Si under wide ranges of annealing temperature and Sn concentration. As a result, low-temperature formation (~300°C) of SiGe(Sn) becomes possible.

2. Experiments and Results

Amorphous $Ge_{1-x}Sn_x$ (x = 0 – 0.26) layers (100 nm thickness) deposited on Si(100) substrates were patterned into island shapes (20 μmφ). After capping SiO_2 layers (1 μm thickness) by sputtering, they were annealed (200 – 1000°C, 1 sec – 170 h) in N_2. The sample structure is schematically shown in Fig.1(b), where the annealing conditions are indicated by hatching in Fig.1(a).

After removing the capping layers, crystal structures of the grown layers were investigated with electron backscattering diffraction (EBSD). The EBSD images of Ge and $Ge_{0.9}Sn_{0.1}$ samples annealed at 650-950°C (1 sec) are shown in Fig.2. For samples without Sn doping, a (100)-oriented layer is obtained after annealing at 950°C (1 sec), which indicates SiGe mixing-triggered melting growth from the Si(100) substrate. This result agrees with our previous study [1-4]. On the other hand, $Ge_{0.9}Sn_{0.1}$ samples indicate (100)-orientated growth in the whole island regions after annealing at temperatures above 800°C (1 sec). It is noted that the growth temperature (800°C) is lower than the melting point of $Ge_{0.9}Sn_{0.1}$ (~890°C).

To investigate composition of grown layers, micro-Raman measurements were performed. The results for Ge and $Ge_{0.9}Sn_{0.1}$ samples are shown in Fig.3(a). In all spectra, Raman peaks due to Ge-Ge bonding are observed. Moreover, Raman peaks due to Si-Ge bonding are clearly observed for annealing temperatures above 950°C and 800°C for Ge and $Ge_{0.9}Sn_{0.1}$ samples, respectively. These SiGe mixing temperatures agree with those for (100)-oriented growth, as shown in Fig.2. Si depth profiles obtained by Auger electron spectroscopy (AES) for $Ge_{0.9}Sn_{0.1}$ samples are shown in Fig.3(b). SiGe with uniform Si concentrations as high as 50–60% is obtained by 800-950°C annealing (1 sec). AES measurements revealed decrease of Sn concentration to ~1%, which was attributed to surface pile-up by segregation during the melt-back process. Analysis of Raman peak positions revealed strain-free of these SiGe(Sn) layers.

To examine effects of Sn concentrations, Raman measurements were performed for samples with various initial Sn concentrations. The results after annealing (1 sec) are shown in Fig.4, where the circles and diamonds indicate that Si-Ge Raman peaks are observed and not observed, respectively. It is found that SiGe-mixing temperatures decrease with increasing Sn concentration. Here, we speculate that SiGe mixing and epitaxial growth starts to occur at interfaces between liquid GeSn regions and Si substrates. These results are attributed to larger fractions of liquid-regions for higher Sn concentrations.

Since epitaxial growth is considered to progress through partially melted regions, we expect that epitaxial growth even at much lower temperatures becomes possible by increasing annealing time. The results

obtained by long-time annealing (1h) are summarized in Fig.5, where open symbols indicate epitaxial growth revealed by EBSD. The growth temperature significantly decreases from 700°C to 550°C by increasing annealing time to 1 h. Amorphous solid-regions in liquid-solid-coexisting GeSn are considered to narrow enough to achieve complete lateral-epitaxial alignment to recrystallized-regions, i.e., previously-melted regions. Detailed analysis is now underway.

Annealing temperatures and times necessary for SiGe(Sn) epitaxial growth are summarized as a function of initial Sn concentration in Fig. 6. As expected, epitaxial growth is achieved at low-temperature of 300°C for initial Sn concentration of 26% by increasing annealing time to 48 h. Sn concentrations in samples grown at low temperatures (≤450°C) were ~2%. Interestingly, it is found that such epitaxial growth was not achieved for the sample (Sn: 26%) at a temperature (200°C) below the solidification point even after very long time annealing (170 h). The fact that growth features are clearly divided by the solidus curve evidences our liquid-solid-coexisting growth model for low-temperature SiGe(Sn) epitaxial growth.

3. Conclusion

Growth features in the liquid-solid coexisting region have been clarified. As a result, low-temperature (~300°C) epitaxial growth of SiGe(Sn) becomes possible. This technique is useful to realize next-generation LSIs, where various multi-functional devices are integrated.

References

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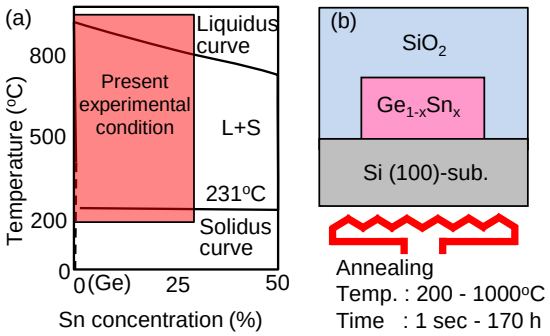

Fig.1. Phase diagram for propose of partial-melting-induced epitaxial-growth in liquid-solid (L+S) coexisting region (a) and schematic sample structure (b).

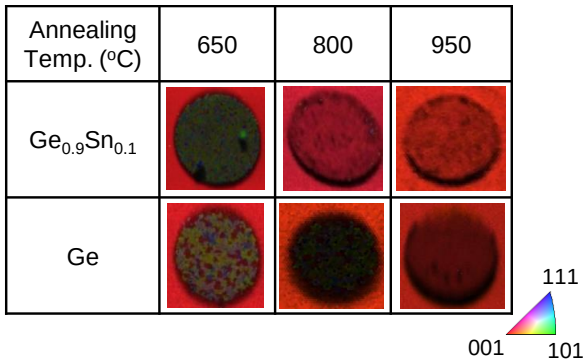

Fig.2. EBSD images of Ge and $Ge_{0.9}Sn_{0.1}$ samples after annealing (650, 800, 950°C, 1 sec).

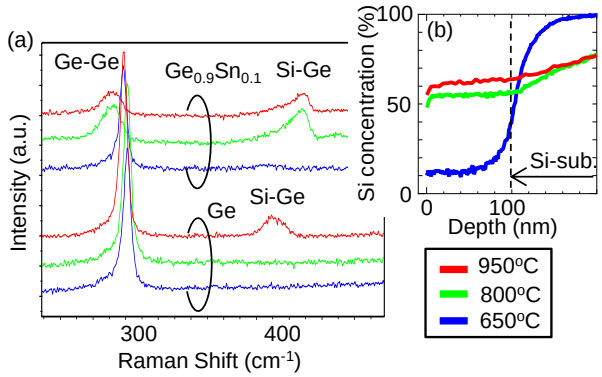

Fig.3. Raman spectra obtained from Ge and $Ge_{0.9}Sn_{0.1}$ samples after annealing (650, 800, 950°C, 1 sec) (a) and depth profiles of Si concentration in $Ge_{0.9}Sn_{0.1}$ samples (b).

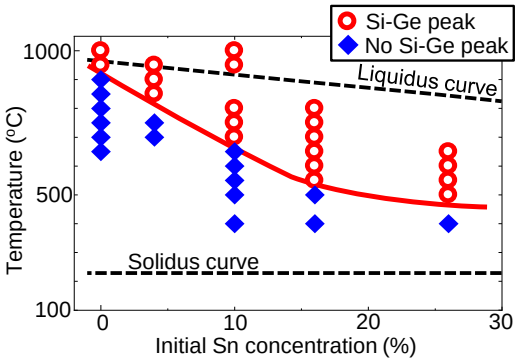

Fig.4. Initial Sn concentration dependence of SiGe mixing after 1-sec-annealing.

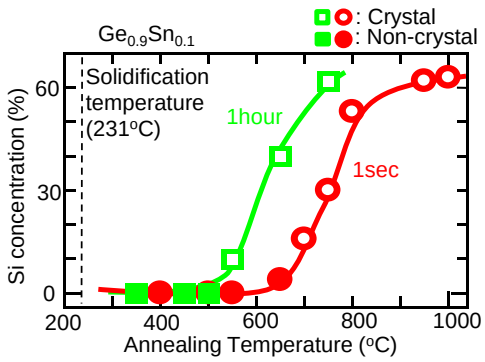

Fig.5. Si concentration as a function of annealing temperature.

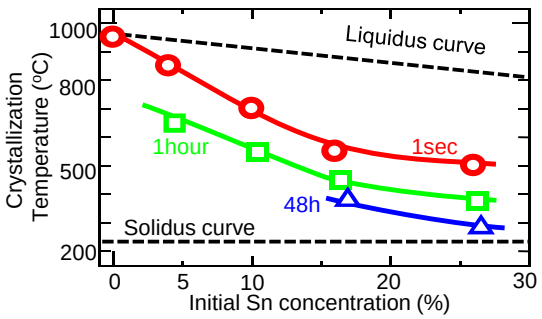

Fig.6. Crystallization temperature as a function of initial Sn concentration.