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Growth of InGaAs single-junction solar cell on GaAs/Ge/Si heterostructure using graded-temperature arsenic technique

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Abstract

The growth of InGaAs single-junction solar cell (SC) on GaAs/Ge/Si heterostructure using graded-temperature arsenic technique, which growth temperature was ramped from 300 to 420℃, is investigated. It is demonstrated that the graded-temperature arsenic technique used on a Ge/Si substrate annealed at 650℃ not only improves the surface morphology but also reduces the anti-phase domains' (APDs) density in GaAs epitaxy (dislocation density: ~$2\times10^{7}cm^{-2}$). Moreover, InGaAs single-junction solar cell was also grown on the GaAs/Ge/Si heterostructure, and energy conversion efficiency is about 9%.

Introduction

Currently, the installation of InGaP/InGaAs/Ge multi-junction solar cells (SCs) is limited by the relatively high cost of III-V solar cells as compared to silicon-based solar cells [1]. Therefore, the integration of the GaAs/Ge/SiGe heterostructure on Si substrates as an alternative template for low-cost III-V based solar cells has attracted much attention [2-3]. However, many growth challenges exist in the GaAs/Ge heterostructure, including anti-phase domains (APDs), misfit dislocations, and the interdiffusion of the Ga, As, and Ge atoms. APD formation in the GaAs/Ge heterostructure can be suppressed by adjusting growth conditions such as the growth temperature, the substrate misorientation angles, and the Ge film annealing process [4-6].

In order to decrease the interdiffusion probability of As and Ge atoms, a low-temperature epitaxial technique and various interfacial layers such as AlAs, Ga, and As were used for the GaAs/Ge heterostructure growth [7-8]. Although a thin AlAs prelayer grown between GaAs and Ge epitaxy suppressed the interdiffusion of Ge atoms, diffusion of Al atoms into the GaAs epitaxy was observed at higher growth temperatures (>540℃) [7]. In contrast, the growth of the Ga prelayer between Ge and GaAs epitaxy decreased the As and Ge interdiffusion as compared to the growth of As prelayer, but the APD formation in GaAs/Ge system was difficult to avoid [8]. Therefore, the development of an advanced technique that can suppress the unwanted interdiffusion while maintaining the lower APD formation in the GaAs/Ge system is necessary for the development of low-cost III-V optoelectronic devices on Si substrate.

Experiment

In this paper, we present the use of an As prelayer grown using graded-temperature technique for the suppression of APD formation. All samples in this study were grown by a low-pressure metal organic chemical vapor deposition (MOCVD, EMCORE D180). Trimethylgallium (TMG), trimethylaluminum (TMAl) and trimethylindium (TMIn) were used as group III sources, whereas arsine (AsH_3) and phosphine (PH_3) were used as group V sources. The precursors for p-type and n-type dopants were carbon-tetrabromide (CBr_4) and dimethyl-telluride (DMTe), respectively. A detailed description of the growth of Ge epitaxy on Si substrate can be found elsewhere [9]. GaAs epitaxy was grown on the Ge/Si heterostructure by a low-temperature epitaxial technique (450℃). The Ge/Si substrate was annealed at 650 ℃ to generate atomic surface steps before the GaAs epitaxial growth [4]. After the GaAs/Ge/Si heterostructure growth, the InGaAs single-junction solar cell was grown subsequently onto alternative substrates, not traditional Ge or GaAs substrates. The structure of InGaAs single-junction solar cell (shown in Figure 1) used in this study includes P-AlGaAs BSF layer, P-InGaAs base layer, N-InGaAs emitter layer, N-InGaP window layer and N^{++}-GaAs contact layer, respectively. On the other hand, the nucleation layer and buffer layer in Fig. 1 are Ge and GaAs epitaxy, respectively.

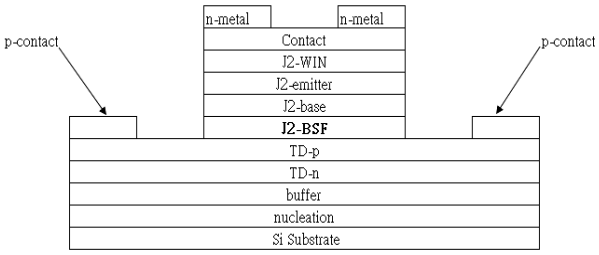

Figure 1. Schematic drawing of InGaAs single-junction solar cell on Si substrate

Results and discussion

Figure 2 shows the TEM images of the GaAs epitaxy (V/III: 20) grown on the Ge/Si heterostructure using a graded-temperature As technique. It can be seen that many APDs were formed in the GaAs layer on the unannealed Ge/Si substrate (threading dislocation density: ~$1\times10^{8}cm^{-2}$), as shown in Fig. 2(a). For the substrate annealed at 650℃, an APD-free GaAs epitaxy with lower dislocation density (10^{6}~$10^{7}cm^{-2}$) was obtained (Fig. 2(b)). These results sug-

gest that, following the short annealing process at high temperature, surface transition may occur on the Ge surface that generates many extra atomic surface steps to provide better As atom coverage [4]. In the selective-area diffraction pattern diffracted from the GaAs/As interface area, only the GaAs diffraction spots exist along [110] zone axis as shown in Fig. 2(b). This observation suggests that the graded-temperature arsenic prelayer does not generate different crystal structure in the GaAs/As epitaxy. This implies that As atom coverage formed on the Ge/Si substrate did not change the structural configuration of GaAs/Ge epitaxy. The As prelayer grown on the Ge/Si substrate annealed at 650℃ modifies the surface morphology of the GaAs epitaxy and reduces the APD formation.

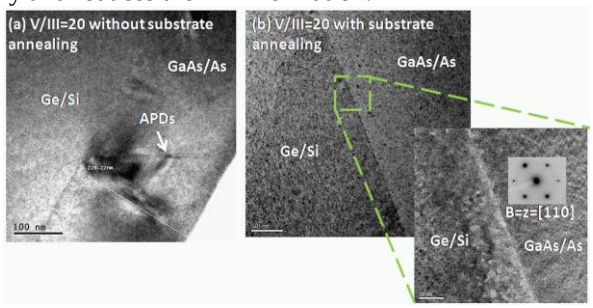

Figure 2. TEM images of GaAs/Ge/Si heterostructure grown at a V/III ratio of 20. (a) unannealed Ge/Si substrate and (b) Ge/Si substrate annealed at 650℃

Figure 3 shows the SIMS depth profiles of Ge, As, and Ga atoms in the GaAs epitaxy grown on the Ge/Si heterostructure using the graded-temperature As technique. It is found that the interdiffusion of Ge into GaAs was suppressed for all the samples. For GaAs epitaxy with a V/III ratio of 20 and the graded-temperature As prelayer on the Ge/Si heterostructure annealed at 650℃, virtually no As interdiffusion was observed as shown in Fig. 3(b). As judged from the SIMS and TEM results, the As prelayer grown using graded-temperature technique is also an excellent candidate for suppressing interdiffusion of the Ga, As, and Ge atoms.

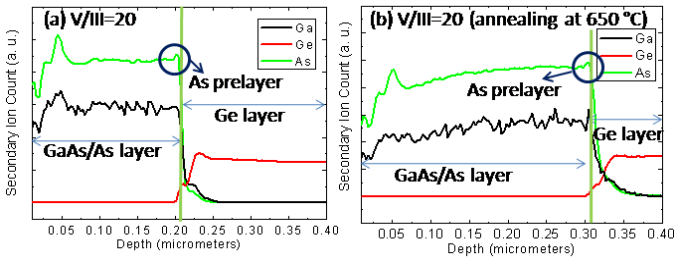

Figure 3. SIMS profiles for GaAs epitaxy grown on a Ge/Si substrate with a graded-temperature As prelayer (a)V/III ratio:20 and (b) V/III: 20 and annealed at 650℃

Figure 4 shows the I-V characteristics of InGaAs single-junction solar cell on GaAs/Ge/Si substrates using graded-temperature arsenic technique. InGaAs single-junction solar cells with Si_3N_4 antireflection coating (ARC) on GaAs/As/Ge/Si heterostructures offer a higher conversion efficiency of 8.6%, which is higher than in states without ARC. Table I shows detailed information for InGaAs single-junction solar cell with ARC on Si substrates demonstrated that I_{sc} value is about 5.6mA, V_{oc} value is about 0.64V, conversion efficiency (EFF) is about 8.6% and Fill factor (FF) is about 68%.

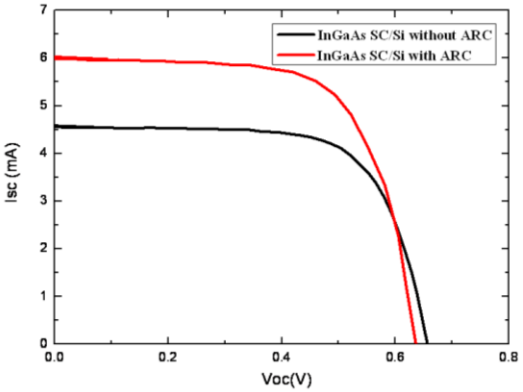

Figure 4. I-V characteristics of InGaAs single-junction solar cell on GaAs/Ge/Si heterostructure

Table 1. Conversion efficiency of InGaAs single-junction solar cell on GaAs/Ge/Si heterostructure

I_{sc} (mA)	5.98174
V_{oc} (V)	0.63637
I_{mp} (mA)	5.23621
V_{mp} (V)	0.49316
P_{mp} (mW)	2.582
P_{opt} (mW/cm^2)	100
EFF (%)	8.568
F.F (%)	67.84

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