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Fabrication of Tri-Gated Junctionless Poly-Si Transistors with Photoresist Trimming Technique

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Abstract

With i-line-based lithography, we've developed a method for fabricating tri-gated junctionless (JL) polycrystalline silicon (poly-Si) transistors having sub-0.1 μm channel length and width. In this approach, the channel length is shrunk with sidewall spacer etching, while the channel width is narrowed with photoresist trimming. Although not optimized yet, the fabricated JL devices exhibit good performance in terms of high on/off current ratio and low subthreshold slope.

1. Introduction

Recently, junctionless (JL) transistors have attracted a lot of attention due to the appealing device performance and the elimination of complicated junction formation process in advanced nano-scale devices [1][2]. Usually in JL devices the channel doping is higher than 10^{19} cm^{-3} which is comparable to that of source/drain of the same doping type. Owing to the abundant carriers contained in the channel, previous works usually adopted a nanowire or an ultra-thin structure as the channel [1-6]. To fabricate JL devices with L smaller or around 100nm, deep-UV steppers or e-beam writers were employed [2-4]. These methods are, however, either high in cost or low in throughput. In this work, we demonstrate the feasibility of using solely i-line-based lithography to fabricate tri-gated JL NW transistors with sub-lithographic channel dimensions.

2. Device Fabrication

Figure 1 shows process flow for fabricating the proposed tri-gated JL transistors. First, a 100nm-thick oxide layer was grown on the Si wafer, and then a 180nm thick in-situ doped n^+ poly-Si layer was deposited and patterned to form two n^+ poly-Si studs, as shown in Fig. 1(a). Next, a 150 nm-thick n^+ poly-Si layer was deposited and etched anisotropically to form the sidewall spacers on the studs, as shown in Fig. 1(b). The above process defines the S/D regions and in-between the channel length (L), which can be readily scaled to or even smaller than 0.1μm. Subsequently, a 10 nm-thick n^+ poly-Si channel film was deposited as shown in Fig. 1(c). Note that the carrier concentration contained in the channel is higher than 10^{19} cm^{-3}. Then, the channel was patterned, followed by the formation of the gate oxide (10 nm) and gate electrode, as shown in Fig. 1(d). To narrow down the channel, a PR trimming step by O_2 plasma was implemented in the aforementioned channel formation process, as shown in Fig. 2.

3. Results and Discussion

Figure 3 shows an SEM image of a device taken after forming the sidewall spacer on S/D studs. L of the device, defined by the spacing between the two studs, is around 0.1μm. Figures 4(a) and (b) displays top view of the JL channels after etching for two devices with L = 0.1 and 0.5μm, respectively. The widths of the two cases are both 93 nm. Transfer curves of the two fabricated JL transistors with gate length of 0.1μm and 0.5μm are respectively shown in Figs. 5(a) and (b). Good device characteristics are obtained, although it can be seen that the subthreshold swing of the JL device with L of 0.1μm is worse than that of long-channel device, so does the DIBL. This is attributed to the rather thick gate oxide. With a further scaling in the oxide thickness, the short channel-effects are expected to be relaxed. Figs. 6(a) and (b) show the output curves of the JL devices with channel length of 0.1μm and 0.5μm, respectively. The output currents of the 0.1um JL device do not saturate at higher drain voltage as shown in Fig. 6(a), owing to the large S/D resistance. Further refinement in S/D formation process is needed to address this issue.

Transfer curves of JL device with channel width of 93nm, 0.2 μm, and 0.5 μm are shown in Fig. 7. It is noticeable that the subthreshold swings of these devices are improved with smaller channel width, owing to better gate controllability. With a reduction in channel width, the device operation shifts from planar to tri-gated configuration. Thus, the subthreshold swing and short channel effect like DIBL are significantly improved with decreasing channel width, as shown in Fig. 8.

4. Conclusion

In this study, tri-gated JL poly-Si NW transistors with both channel length and width down to 0.1μm were fabricated by a method which involved only i-line-based lithography. This method combines sidewall-spacer etching and PR trimming techniques to shrink the channel dimensions. The fabricated JL devices show excellent electrical performance with high on/off current ratio and good subthreshold slope.

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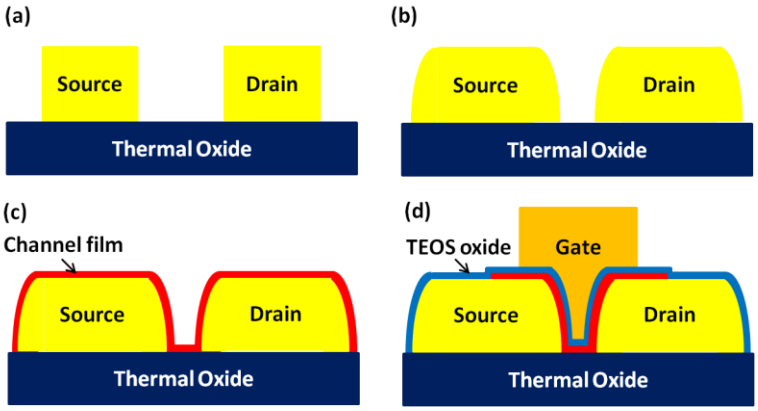

Fig. 1 Illustrations of main process steps for fabrication of JL devices.

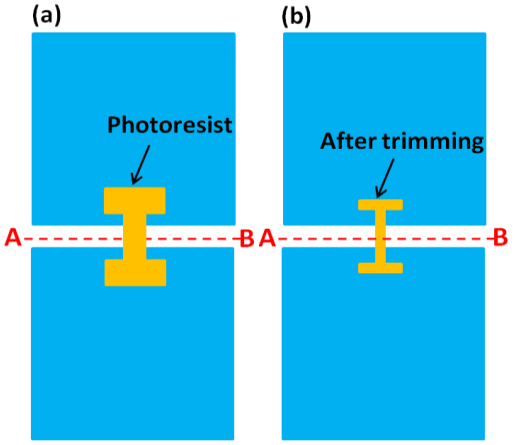

Fig. 2 Illustrations of channel formed by PR trimming.

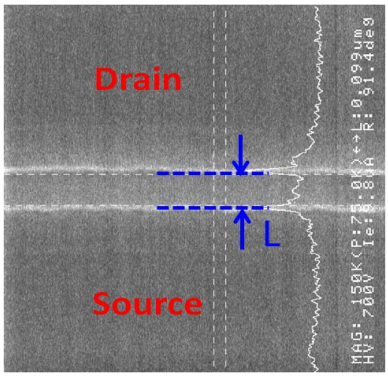

Fig. 3 Top view of a device taken after sidewall spacer etching. L is 0.1μm.

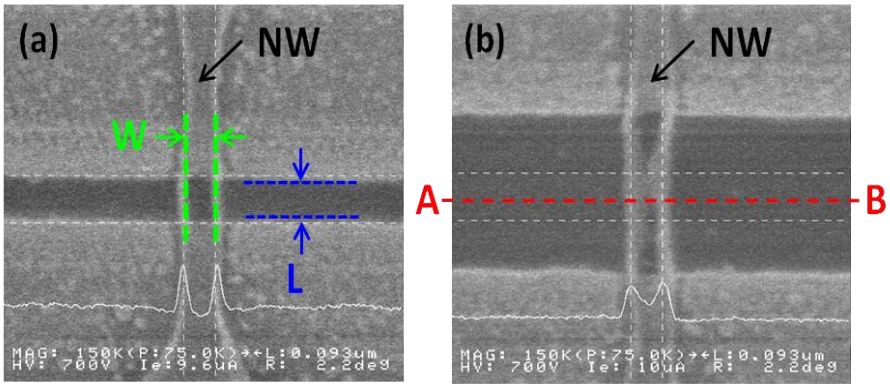

Fig. 4 SEM images of the channel of JL devices with L of 0.1μm and 0.5μm, respectively. The width of the resulted nanowire (NW) channel is 93 nm.

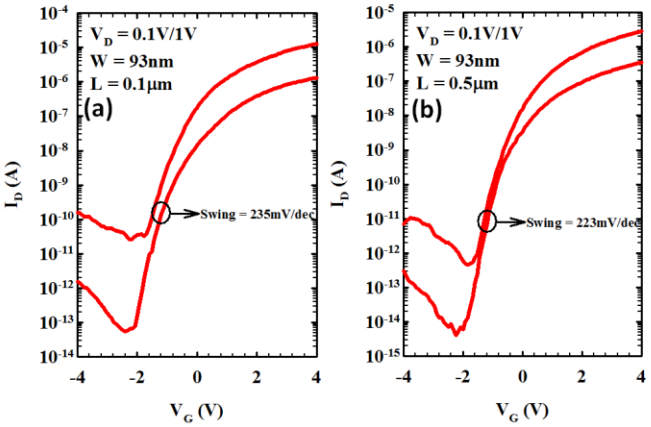

Fig. 5 Transfer curves of JL devices with L of 0.1μm and 0.5μm, respectively.

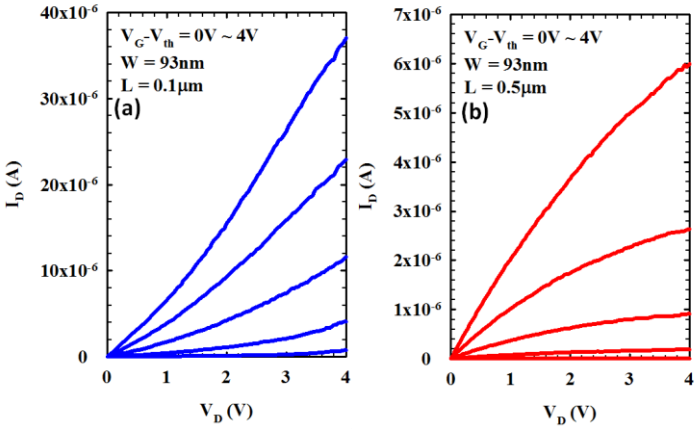

Fig. 6 Output curves of JL devices with L of 0.1μm and 0.5μm, respectively.

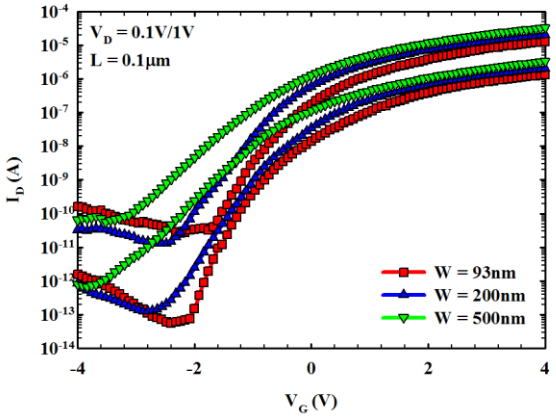

Fig. 7 Transfer curves of JL NW devices with width of 93nm, 0.2 μm, and 0.5 μm, respectively.

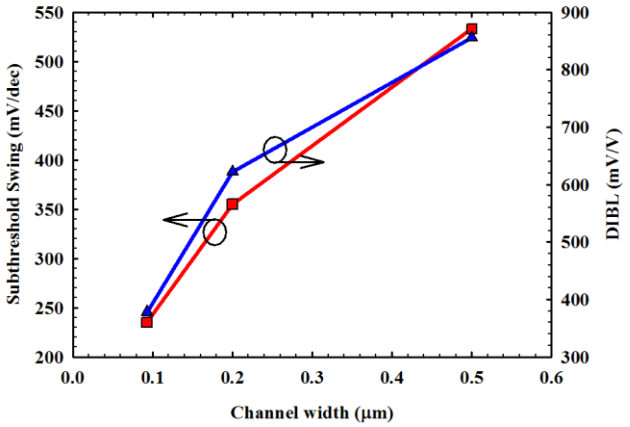

Fig. 8 Subthreshold swing and DIBL as a function of channel width.