Ultrathin GeOₓ Interfacial Repairer Formed by Thermal Oxidation for Germanium MOS Devices

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Abstract

A thermal oxidation method with a thin Al₂O₃ film employed as oxygen blocking layer has been proposed to form an ultrathin GeOₓ interfacial repairer for better interface quality. Also the thin Al₂O₃ layer performs well to inhibit GeO desorption from the GeOₓ/Ge interface during thermal treatment. MOS capacitors and MOSFETs fabricated with the engineered Al₂O₃/GeOₓ/Ge gate stacks exhibit good electrical characteristics.

1. Introduction

Utilizing high-κ gate stacks is a promising way to realize high performance Ge MOSFETs, which desires for low interface trap density (Dₓ). Many efforts such as sulfur passivation[1] and Si passivation[2] have been made to reduce Dₓ at high-κ/Ge interface. However, forming a thin GeOₓ interfacial repairer (IR) between high-κ dielectrics and Ge is one of the best solutions to improve interface quality.[3] It is significant to scale down the thickness of GeOₓ layer due to its low κ value. R. Zhang et al. have employed plasma post oxidation to get ultrathin GeOₓ IR and maintained 1nm EOT gate stack[4]. Nevertheless, the most fundamental method to get GeOₓ layer is thermal oxidation, which really needs a better thickness control. In this paper, to achieve a thin GeOₓ IR, we employed a thin Al₂O₃ film as oxygen blocking layer to suppress oxygen diffusion and reaction at Ge surface. Also the thin Al₂O₃ layer performs as a diffusion barrier to inhibit surface damage causing by the GeO desorption. MOS capacitors (MOSCAPs) and MOSFETs were fabricated to study the Al₂O₃/GeOₓ/Ge gate stacks.

2. Experimental

A 1.5nm-thick Al₂O₃ film was deposited on the pre-cleaned Ge wafer by atomic layer deposition (ALD) at 300°C. Thermal oxidation was carried out inside a furnace at atmospheric pressure in pure oxygen ambient at 550°C for 60s. The second-round 3nm Al₂O₃ layer was deposited on the Al₂O₃/GeOₓ/Ge samples by ALD. Post-deposition annealing (PDA) at 550°C for 10min and low-temperature oxygen annealing (LOA) at 400°C for 30min were performed to improve the dielectric quality and further stabilize the GeOₓ/Ge interface[5,6]. For the MOSCAPs, Ti/Au (20/200nm) top electrodes and Al (300nm) back contact were deposited by metal evaporation. The Ge p-MOSFETs were fabricated on n-type Ge substrate using the same dielectric stacks fabrication flow of Ge MOSCAPs above mentioned. The main process flow of Ge p-MOSFETs with gate-first fabrication method is shown in Fig. 1.

3. Results and discussion

Figure 2(a) shows the reaction constant (redox reaction) for various candidate dielectric oxides on Ge surface, and figure 2(b) shows the thermal desorption spectroscopy (TDS) results of GeO desorption for (i) Al₂O₃/Ge and (ii) GeO₂/Ge. We can conclude that Al₂O₃ works as a better diffusion barrier for its better thermal stability on Ge and no GeO desorption during thermal oxidation. T. Tabata et al. also have proved that Al₂O₃ films can suppress the GeO desorption from the Al₂O₃/GeO₂/Ge stack even at high temperature[7].

Fig. 1 Main process flow of MOSFETs with gate-first fabrication method.

Fig. 2 (a) Reaction constant (redox reaction) for various candidate dielectric oxides on Ge. (b) TDS spectra of GeO desorption from Al₂O₃/Ge and GeO₂/Ge stacks.
Transmission electron microscope (TEM) was carried out on the MOSCAPs to determine the GeOₓ thickness in the final gate stack structure, as illustrated in Fig. 3. After the thermal oxidation at 550°C for 60s, the GeOₓ thickness is approximately 0.5nm, which demonstrates the effectiveness of an AlₓOᵧ oxygen blocking layer in scaling down the GeOₓ IR thickness.

Electrical characterization of MOSCAPs was analyzed to investigate the electrical quality of the scaled GeOₓ IR. Figure 4(a) shows C-V characteristics of MOSCAPs with 0.5nm GeOₓ and 4.5nm AlₓOᵧ. The accumulation capacitance is 1.2µF/cm², indicating that the capacitance equivalent thickness (CET) is ~2.1nm. Well-behaved C-V curves are shown with a small frequency dispersion at flat band voltage (V_{FB}=0.1V) and the hysteresis at 1MHz is about 50mV. Also a low gate leakage is shown in Fig. 4(b), about 5×10⁻⁸A·cm⁻² at V_{G}=V_{FB}+1V.

Fig. 4 C-V curves and leakage current of n-type MOSCAPs with 4.5nm AlₓOᵧ.

A low-temperature conductance method was taken advantage of to quantitatively observe the impact of the GeOₓ interfacial repairer on Dₜ at the AlₓOᵧ/GeOₓ/Ge interface. Figure 5 shows the Dₜ spectrum estimated by the conductance method at 160K (~1×10¹⁵cm⁻² at Ei=0.25eV), in comparison with the previously reported data by other group[3].

Figures 6(a) and 6(b) show the typical output (Iₒ-Vₒ) and transfer (Iₚ-Vₒ) characteristics of Ge (100) p-MOSFETs with a channel width/length of 200µm/6µm. The Iₒ/Iₚ ratio at room temperature is above 1×10⁴. And a subthreshold slope of 115mV/dec was achieved, indicating a small Dₜ of p-MOSFETs.

Fig. 6 (a) Iₒ-Vₒ and (b) Iₚ-Vₒ of the Ge (100) p-MOSFETs with AlₓOᵧ/GeOₓ/Ge gate stack.

4. Conclusions

In conclusion, the thin AlₓOᵧ film serves well as an oxygen blocking layer to scale down the GeOₓ IR thickness and a protecting layer to suppress the GeOₓ desorption. Thin GeOₓ IR contributes to achieve high quality interface, which has nearly no impact on the EOT simultaneously. Other high-k dielectrics such as HfO₂ and La₂O₃ can take place of the second-round AlₓOᵧ layer to get better properties of gate stacks. The improved thermal oxidation method needs further optimization and will provide a potentiality for Ge MOS device.

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References