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Thermal Stability of Short Channel, High-Mobility Organic Thin-Film Transistors having Bottom-Contact Configuration

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Abstract

Thermal stability of alkylated-DNTT thin-film transistors (TFTs) has been investigated. Although the properties of the TFTs degraded even for storage at room temperature, the annealing at 120 °C after the degradation improved the properties toward those at early stage. The annealed short-channel TFTs exhibited mobilities of 1.9 to 2.6 cm^2/Vs.

1. Introduction

Since high field-effect mobilities up to 7.9 cm^2/Vs were reported, alkylated dinaphthothienothiophene (Cn-DNTT) has been a promising material for high mobility p-channel organic thin-film transistors (TFTs) [1]. Some groups have realized such high mobilities in TFTs with C_{10}-DNTT as channel materials [2-4]. However, such high mobility demonstrated in long-channel transistors having top-contact configuration. On the other hand, bottom-contact configuration is desirable for short-channel transistors and the high frequency operation. This is because short-channel transistors with bottom-contact configuration are easily realized by conventional photolithography.

We have demonstrated bottom-contact pentacene TFTs operating at high frequencies above 10 MHz [5]. Gold/AuNi drain/source electrodes modified with pentafluorobenzenethiol (PFBT), which are effective to reduce contact resistance, were used to realize the short-channel, high-mobility pentacene TFTs [6]. The modified electrodes are effective for C_{10}-DNTT TFTs as well as pentacene TFTs [7].

DNTT-based TFTs have exhibited high stability to storage in air [8]. On the other hand, it was reported that the mobilities of C_{10}-DNTT with top-contact configuration slightly decrease with storage time [3]. The cause of the degradation for C_{10}-DNTT has been not clear.

In this work, we report thermal stability of short-channel, high-mobility C_{10}-DNTT TFTs having bottom-contact configuration. The performance of the TFTs as-fabricated, stored and annealed is discussed.

2. Experimental

Figure 1 shows cross-section of the C_{10}-DNTT TFT fabricated in this work. The chemical structure of C_{10}-DNTT is shown in the inset in Fig. 1. A silicon substrate with a 35-nm-thick SiO_2 layer was used as a substrate of the TFT. The SiO_2 has a unit area capacitance of 92.3 nF/cm^2. Drain/source electrodes of Au/AuNi modified with PFBT were used to reduce contact resistance. The contact electrodes were patterned by photolithography and lift-off. The SiO_2 surface was treated with hexamethyldisilazane. C_{10}-DNTT was deposited through a metal mask on a substrate heated at 100 °C. The channel width (W) was 1 mm and the channel length (L) was in the range of 2 to 40 µm. The current-voltage characteristic was measured in a dry-nitrogen glove box.

The TFTs were stored in the glove box for about two weeks. To investigate the thermal stability, the TFTs were annealed at 120 °C for about 15 min after the storage of two weeks. Furthermore, the TFTs were annealed at 140 °C for about 15 min. The current-voltage characteristic was measured at each step.

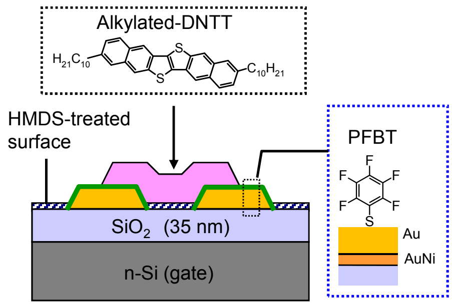

Fig. 1 Schematic illustration of a bottom-contact C_{10}-DNTT TFT.

3. Results

Figure 2 shows drain current (I_D) versus gate voltage (V_G) characteristics of a C_{10}-DNTT TFT with L = 4 µm. The characteristics shows the results measured for the TFT as-fabricated, stored for two week, and annealed at 120 °C. The current dramatically decreased even for storage at room temperature in nitrogen for two weeks as seen in Fig. 2. The I_D–V_G characteristic exhibits an abnormal curve in the range of low voltages. The square root of $|I_D|$ non-linearly increases with V_G. On the other hand, the annealing at 120 °C improved the current characteristics. Although the sloop of $|I_D|^{1/2}$-V_G curve for the annealed TFT is slightly low as compared to that for the fabricated TFT, the on current dramatically improves.

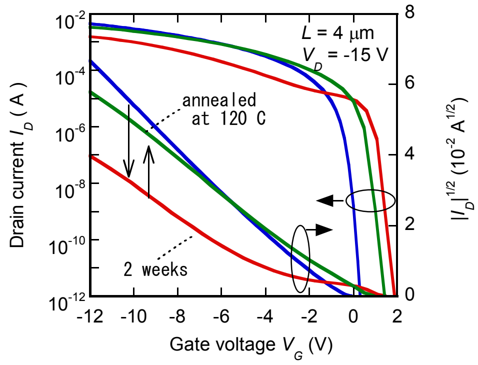

Fig. 2 Transfer characteristics of a C_{10}-DNTT TFT for (a) the as-fabricated TFT, (b) the TFT stored for two weeks, and (c) the TFT annealed at 120 °C after two-week storage.

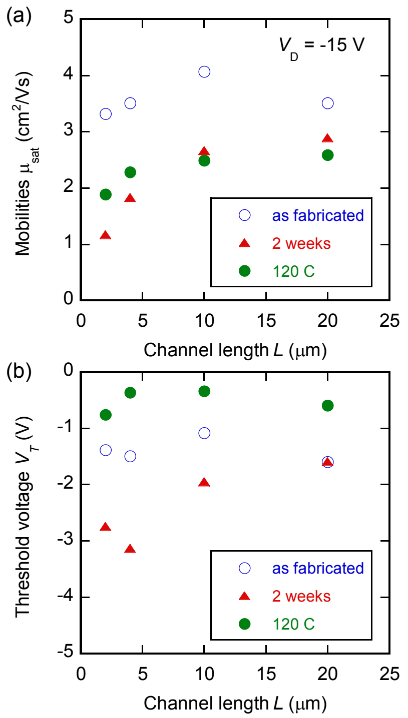

Fig. 3 Channel length dependence of mobilities in the saturation regime and threshold voltages of C_{10}-DNTT TFTs.

The mobilities (μ_{sat}) and threshold voltage (V_T) of C_{10}-DNTT TFTs with different channel lengths are summarized in Fig. 3. The values were estimated by fitting a line to the $|I_D|^{1/2}$-V_G curve at a drain voltage (V_D) of -15 V. The mobilities for the stored TFTs decrease for all channel length. In particular, the degree of the decrease is very large in the short-channel TFTs. For the TFT with L = 2 µm, the mobility decreases from 3.3 cm^2/Vs to 1.2 cm^2/Vs. In addition, the storage for two weeks leads to increase in the absolute value of threshold voltage $|V_T|$. On the other hand, the annealing improve the mobility for the shot channel TFTs of L = 2 and 4 µm. In addition, the $|V_T|$ values shift to zero voltage. The changes in μ_{sat} and V_T are large in the short channel TFTs. The behavior implies that the storage increases the contract resistance and the annealing suppresses the resistance.

Figure 4 shows change of mobilities and on-current of the C_{10}-DNTT TFT with L = 4 µm. The on-current represents drain current at V_G = -12 and V_D = -15 V. The mobility decreases even at storage of one week. Although the annealing at 120 °C leads to increase in the mobility, the annealing at 140 °C causes decrease in the mobility.

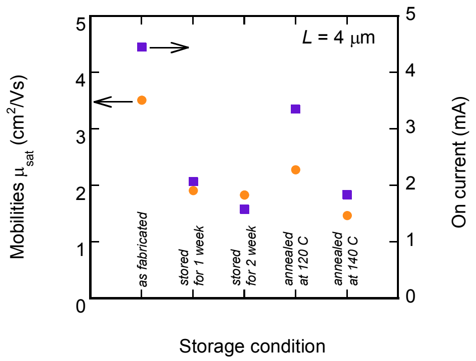

Fig. 4 Change of mobilities and on-current of the C_{10}-DNTT TFT.

4. Conclusions

We investigated thermal stability of C_{10}-DNTT TFTs with bottom-contact configuration. The properties of the TFTs stored in a nitrogen-filled glove box at room temperature degraded even for the brief period of a few days. On the other hand, annealing at 120 °C after the degradation improved the properties toward those at early stage. The annealed TFTs have mobilities of 1.9 to 2.6 cm^2/Vs. However, annealing at 140 °C leaded to further degradation. These results suggest the existence of optimal annealing condition for high performance.

Acknowledgements

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