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Device performance of top-gate organic transistors with embedded electrodes: Effects of thin and planar C_8-BTBT layer on FET characteristics

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Abstract

Top-gate organic FETs with embedded source-drain electrodes using the solution-processable organic semiconductor of 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene have been fabricated to investigate the effect of the planarization of semiconductor. The top-gate devices with embedded electrodes exhibit higher mobilities with smaller device-to-device variations than those with conventional non-embedded electrodes. Moreover, the devices with embedded electrodes show good characteristics even using thinner semiconductor layers.

1. Introduction

Solution-processable small-molecule semiconductors have attracted increasing interest for the fabrication of high-performance organic field-effect transistors (OFETs) using low-cost solution processes. Among them, 2,7- dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C_8-BTBT) have received considerable attention owing to its high carrier (hole) mobility and high air stability, and high field-effect mobilities of 0.46–1.80 $cm^2V^{-1}s^{-1}$ have been reported in C_8-BTBT FETs processed using a conventional spin-coating technique [1]. Moreover, it has been shown that extremely high mobilities ranging from 5 to 31.3 $cm^2V^{-1}s^{-1}$ can be achieved by forming single crystalline C_8-BTBT films via various crystal growth techniques [2-4].

Besides the improvement of field-effect mobility, the increase in the reliability of C_8-BTBT FETs is also important for practical application. In previous study, we have reported that the use of a top-gate and bottom-contact (TGBC) configuration with soluble fluoropolymer gate insulators enables the reproducible fabrication of C_8-BTBT FETs with high mobility, low threshold voltage, and high electrical stability despite using spin coating [5]. TGBC configurations have the advantages of the improvement of carrier injection and of the miniaturization of source-drain electrodes. However, steps formed between source-drain electrodes and substrate generally prevent the planarization and thinning of organic semiconductor layers, and a decrease in field-effect mobility and an increase in device-to-device variation due to the electrode steps have been reported in OFETs with bottom-gate and bottom-contact configurations [6,7].

In this study, we fabricate top-gate C_8-BTBT FETs with embedded source-drain electrodes and investigate the effect of the planarization and thinning of organic semiconductor layers on the electrical performance of the top-gate C_8-BTBT FETs.

2. Experiments

Figure 1(a) shows the schematic illustration of fabricated top-gate C_8-BTBT FETs with embedded source-drain electrodes. The embedded source-drain electrodes were fabricated by photolithography processes. After photoresist patterns were formed on the cross-linked poly(4-vinyl phenol) (PVP) layer, uncovered PVP layers were removed by dry etching. Then, Cr and Au were sequentially deposited on the top of the substrate, followed by lift off of the photoresist layer. An atomic force microscope (AFM) image of a fabricated substrate with embedded electrodes is shown in Fig. 1(b). The planer substrates with electrode steps less than 10 nm can reproducibly be fabricated by the present technique. The organic semiconductor and gate insulator layers were prepared by spin coating of organic solutions of C_8-BTBT and CYTOP, respectively. Finally, Al gate electrodes were defined on the CYTOP layer by vacuum evaporation using a shadow mask.

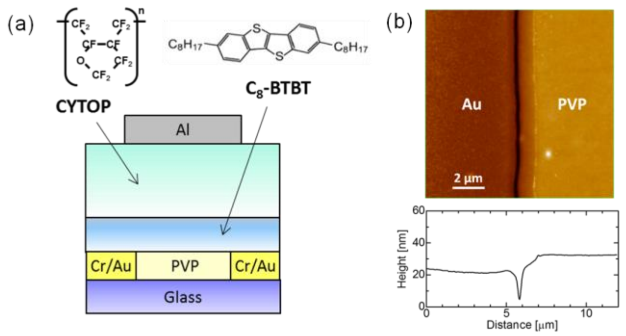

Fig. 1. (a) Device structure of top-gate C_8-BTBT FETs with embedded source-drain electrodes. (b) AFM image and height profile of a fabricated substrate with embedded electrodes

3. Results and discussion

Figure 3 shows typical transfer and output characteristics of top-gate C_8-BTBT FETs with embedded source-drain electrodes. For comparison, the electrical characteristics of top-gate devices with conventional (non-embedded) electrodes fabricated on glass surfaces are also shown. Top-gate C_8-BTBT FETs with embedded electrodes show good performance with low threshold voltages and negligible hysteresis as well as conventional devices. The maximum mobility obtained from devices with embedded electrodes having channel length of 250 µm is 4.9 $cm^2V^{-1}s^{-1}$, which is higher than that of conventional devices (3.7 $cm^2V^{-1}s^{-1}$). The improvement of mobility is mainly caused by the enhancement in the crystallization of C_8-BTBT films on hydrophobic PVP layers.

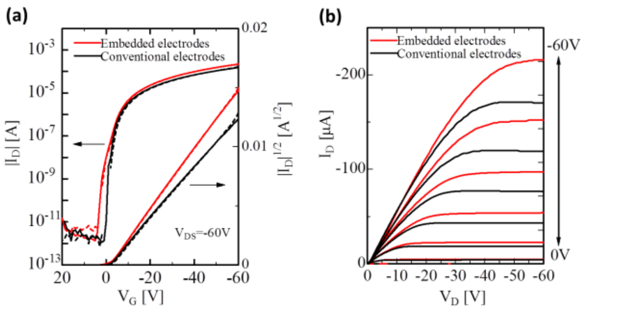

Fig. 3. (a) Transfer and (b) output characteristics of top-gate C_8-BTBT FETs with embedded and conventional electrodes. Channel length is 250 µm.

To clarify the effect of planarization of C_8-BTBT layers, we fabricated top-gate C_8-BTBT FETs with conventional electrodes on PVP buffer layers and compared with devices with embedded electrodes, as shown in Fig. 4. We see that top-gate C_8-BTBT FETs with embedded electrodes exhibit higher field-effect mobilities than devices with conventional electrodes, which becomes pronounced as the channel length is reduced. It is also seen that the mobilities of devices with embedded electrodes show smaller device-to-device variations as compared to those with conventional electrodes.

The obtained results clearly indicate that the carrier injection of top-gate C_8-BTBT FETs is improved by the planarization of C_8-BTBT layers since the increase in the contribution of contact resistance to the total resistance of devices results in an apparent decrease in the field-effect mobility of short-channel devices [5]. The typical contact resistance of the devices with the embedded electrodes estimated using the transmission line method is 4 kΩcm, which is smaller than that of the device with conventional electrodes (10 kΩcm). The smaller disorder at electrode steps due to the planarization of C_8-BTBT layers would be responsible for the reduced variation in the field-effect mobilities of the devices with embedded electrodes.

Finally, we study the influence of thinning of semiconductor layers on top-gate C_8-BTBT FETs with embedded electrodes and conventional electrodes. By thinning C_8-BTBT layers, the mobilities of devices with conventional electrodes are greatly decreased, as a result of the decrease in carrier injection. On the other hand, devices with embedded electrodes show good performance with high mobilities.

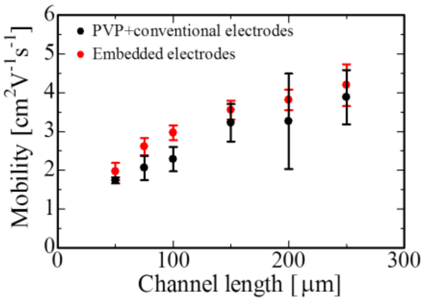

Fig. 4. Channel length vs. field-effect mobility of top-gate C_8-BTBT FETs with embedded electrodes and conventional electrodes prepared on PVP buffer layers.

4. Conclusions

We have fabricated top-gate C_8-BTBT FETs with embedded source-drain electrodes to investigate the effect of the planarization of organic semiconductor layers on the electrical characteristics. The top-gate devices with embedded electrodes show good performance and small device-to-device variations in field-effect mobilities, and the maximum field-effect mobility is 4.9 cm^2/Vs. We also found that the mobilities of short-channel devices are improved using embedded electrodes, as a result of the decrease in contact resistance. In addition, the fabrication of top-gate C_8-BTBT FETs with thin semiconductor layers using embedded electrodes was demonstrated.

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