

Surface Modification of Self-Assembled Monolayers for Organic Transistors

Shigeyoshi Ito^{1,2}, Sung Won Lee^{1,2}, Tomoyuki Yokota^{1,2}, Takeyoshi Tokuhara^{1,2}, Hagen Klauk³, Ute Zschieschang³, Tsuyoshi Sekitani^{1,2} and Takao Someya^{1,2}

¹The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8654, Japan
Phone: +81-3-5841-0411 E-mail: itou@ntech.t.u-tokyo.ac.jp

²Exploratory Research for Advanced Technology (ERATO), Japan Science and Technology Agency (JST)

³Max Planck Institute for Solid State Research, Heisenbergstrasse 1, 70569 Stuttgart, Germany.

Abstract

We have fabricated DNTT organic thin-film transistors (OTFTs) using self-assembled monolayers (SAM) based on phosphonic acids in the gate dielectric. The surface of SAM has been modified by novel modification method of DUV parallel ray exposing system. We have investigated the relationship between the surface property of SAM and electrical performance of OTFT. Maximum OTFT mobility of 1.6 cm²/Vs was obtained without modification. Meanwhile, wettability of SAM was significantly improved by the modification. This hydrophilic surface of SAMs enables us to deposit solution-semiconductor on SAMs gate dielectric layer by drop-casting method.

1. Introduction

Organic thin-film transistors (OTFTs) have received large amount of interest in these days. It is because its semiconducting layer can be deposited with solution processing. Many studies have been made about solution processed OTFTs but it is very difficult to operate solution processed OTFTs in low operational voltage and low power consumption. To drive OTFTs in low operational voltage and low power consumption, using self-assembled monolayers (SAM) in the gate dielectric layer was reported[1]. In the report, circuits using OTFTs were operated in the supply voltage of as low as 1.5 V.

However, combination of these two factors, depositing semiconducting materials on the SAM surface with printing method, does not be achieved. The main problem with existing approach for applying printing techniques to SAM gate dielectrics is the surface property of SAM. SAM makes very dense surface and has low surface energy; therefore, the surface of SAM is hydrophobic. Because of this hydrophobic surface, gate dielectric of SAM sheds the ink of semiconductor. There are some research about modifying SAM surface with many kinds of method such as ion beam[2], electron beam[3], DUV photon beam[4], and so on. However, all of them has problems when we think of applying it to solution processed transistor with SAM gate dielectric.

To realize fabricating OTFTs with solution-processable organic semiconductors on the gate dielectric of SAM, we have developed a novel modification method for SAMs. With the treatment, we successfully

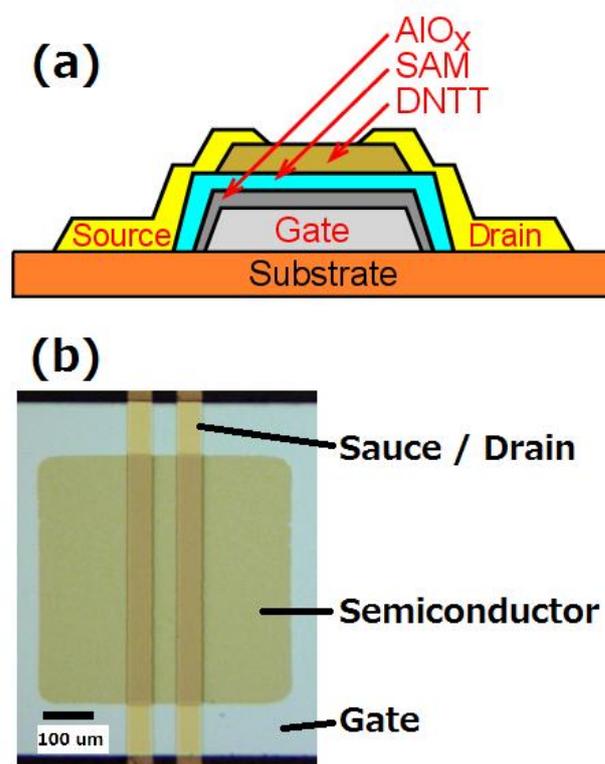


Fig. 1 (a) A schematic illustration of our OTFT (b) A microscopic image of fabricated device with channel length of 38 μm and channel width of 500 μm.

modified the surface of SAM gradually. Mobility was changed from 1.6 cm²/Vs which is the value of non-treated OTFTs to 0.1 cm²/Vs which is the value of treated OTFTs for 20 minutes. This gradual change of mobility implies SAM can be modified without totally removing it by using our DUV exposure equipment. This result will enable us to deposit semiconductor on SAM with solution processing method.

2. Experiments

DUV exposure equipment

To modify the surface, we have invented a novel Deep Ultra-violet (DUV) exposure equipment. It consists of DUV light source and parabolic mirror. The wavelength of the light is around 180 nm, which is lower than

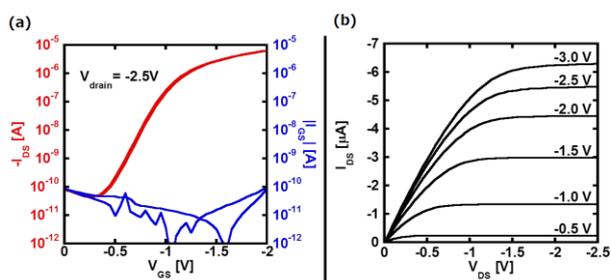


Fig. 2 Transistor characteristics of DNTT OTFT without DUV treatment (a) Transfer characteristics (b) Output characteristics

the wave length of conventional DUV exposing system (which is around 300 nm). In addition, by placing the light source at the focus of its parabolic mirror, we obtained parallel ray of DUV, which enables us to make fine pattern on the surface.

Fabrication Process

The schematic illustration of our top-contact OTFT is shown in Fig. 1(a). These transistors are fabricated by vacuum evaporation, plasma ashing, dipping processes, and exposing process. First, a 50-nm-thick Al layer is thermally evaporated on a polyimide substrate the thickness of which is 75 μm through a shadow mask to form gate electrode. Then, AlO_x was deposited on the gate electrodes by plasma ashing. On this AlO_x layer, only 2-nm-thick SAM layer was formed by dipping to SAM solution, which consists of N-Octadecylphosphonic acid and 2-propanol. as a p-type or n-type organic semiconductor channels. Following the formation, surface of SAM layer on some devices was exposed to DUV light for 5 min to 20 min. After that, 30-nm-thick DNTT (dinaphtho[2,3-b:2',3'-f]thieno [3,2-b]thiophene) was deposited by vacuum evaporation with a shadow mask. Finally, Au lines were patterned evaporated by thermal evaporation process for source and drain electrode. Fig. 1(b) shows a microscopic image of the fabricated devices. The TFTs have a channel length of 38 μm and a channel width of 500 μm .

3. Result

Fig. 2 shows electrical properties of fabricated OTFT without DUV treatment with channel length and width of 38 μm and 500 μm respectively. The mobility of 1.6 cm^2/Vs was calculated from transfer characteristics shown is Fig. 2 (a) and on/off current ratio is 10^6 .

Then, we measured electrical property of OTFTs which has treated SAM layer with DUV light for 5 and 20 min and calculated mobility in the same way described above. The result is shown in Fig. 3. The mobility was decreased from 1.6 cm^2/Vs to 0.1 cm^2/Vs .

4. Conclusions

We have manufactured high performance organic TFTs with SAM layer in the gate dielectric and successfully modified the surface of SAM and calculated the

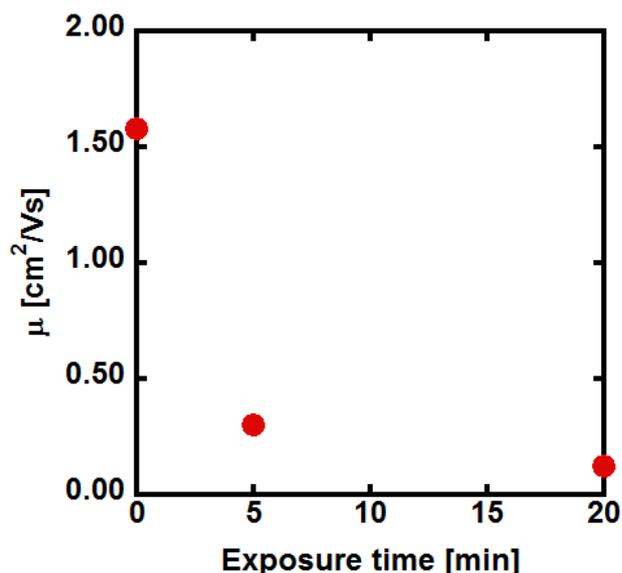


Fig. 3 Mobility change of DUV exposed OTFTs. Three kinds of transistor was measured. First one is non-treated, second one is exposed for five min and third one is exposed for 20 min. Mobility is about 1.6 cm^2/Vs , 0.3 cm^2/Vs and 0.1 cm^2/Vs respectively.

mobility of each transistors. From the result, we confirmed that our exposure equipment can modify the surface of SAM layer gradually, which enables us to deposit semiconductor layer with drop-casting method on the SAM layer without totally removing SAM. This result implies that we will be able to fabricate OTFTs with SAM layer by printing techniques.

Acknowledgements

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References

- [1] H. Klauk, U. Zschieschang, J Pflaum and M. Halik, *Nature*. **445** 745 (2007).
- [2] A. Rezaee, A. K. A. Aliganga, L. C. Pavelka and S. Mittler, *PCCP* **12** 4104 (2010).
- [3] N. Ballav, S. Schilp and M. Zharnikov, *Angew. Chem.* **120** 1443 (2010).
- [4] S. K. Park, D. A. Mourey, S. Subramanian, J. E. Anthony and T. N. Jackson, *Adv. Mater.* **20** 4145 (2008).