# Design of a Three-Terminal MTJ-Based Nonvolatile Logic Element with a 2-ns 64-Bit-Parallel Reconfiguration Capability 

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#### Abstract

A 6-input nonvolatile logic element (NVLE) using threeterminal magnetic tunnel junction (3T-MTJ) devices is presented for low-power and real-time reconfigurable logic LSI applications. Since the write current path of a 3T-MTJ device is separated from its read current path and its resistance value is quite small, multiple 3T-MTJ devices can be reprogrammed simultaneously in parallel, which results in real-time logic-function reconfiguration within a few nanoseconds. Moreover, by merging a circuit component between combinational and sequential logic functions, transistor counts can be minimized. As a result, 2-ns 64-bit-parallel circuit reconfiguration is realized by the proposed $\mathbf{6}$-input NVLE with $\mathbf{6 6 \%}$ of transistor counts reduction, compared to those of a conventional CMOS-based one.


## 1. Introduction

A nonvolatile field-programmable gate array (NVFPGA) using magnetic tunnel junction (MTJ) devices is one promising solution for low power and reconfigurable logic LSI applications since an MTJ device has attractive features such as virtually unlimited endurance and 3-D stacking capability [1]. By combining spin-transfer-torque (STT) MTJ devices with logic-in-memory structure where logic function and nonvolatile storage function are compactly merged [2], a nonvolatile logic element (NVLE), which is a fundamental component of the NVFPGA, is presented [3]. However, since both read current and write current flow the same path in the STT-MTJ device, write current must be applied via high MTJ resistance and long-time serial reconfiguration is unavoidable, which limits application of the NVLE to statically reconfigurable logic [4].
In this paper, an NVLE using three-terminal MTJ (3T-MTJ) devices is presented not only for statically reconfigurable logic but also dynamically one. Since the write current path of a 3T-MTJ device is separated from the read current path and its resistance has a quite small constant value compared to that of MTJ resistance [5], sufficient write current can be applied to each of several dozens of 3T-MTJ devices simultaneously in parallel. Therefore, a dynamic reconfiguration is applicable in the proposed NVLE. Moreover, since a single-ended sense amplifier [6] in the proposed NVLE is shared between a nonvolatile lookup table (NVLUT) circuit and a nonvolatile flip-flop (NVFF), total transistor counts are minimized. These attractive features of the proposed NVLE are described in the following section.

## 2. 3T-MTJ-Based Nonvolatile Logic Element

Figure 1 (a) shows a 3T-MTJ device where domain-wall motion (DWM) is utilized [5]. If the spin directions of the reference layer and the DWM layer are parallel, the resistance $R_{M}$ takes a low value $R_{P}$, and if they are anti-parallel, $R_{M}$ takes a high value $R_{A P}$. The magnetization state can be programmed by applying bi-directional write current $I_{W R}$ between T2 and T3 whose resistance value is less than $150 \Omega$. Thus, the 3T-MTJ device can be regarded as a variable resistor which stores binary data $Y$ as a resistance value as shown in Fig. 1 (b).
Figure 2 (a) shows a block diagram of the proposed 2-input NVLE which is mainly composed of an NVLUT circuit and
an NVFF to create a structure capable of implementing either combinational logic or sequential logic. The NVLUT circuit is implemented based on single-ended circuitry which makes the NVLUT circuit compact [6]. Since the singleended sense amplifier is also used as a latch to hold output data of the NVLUT circuit, sequential logic can also be implemented by cascading just only one nonvolatile latch which is implemented using standard CMOS FF together with two complementary 3T-MTJ devices. Figure 2 (b) shows a 3TMTJ configuration array of the 2 -input NVLE where a large sized write-control transistor is shared among all the configuration cells. Since sufficiently high current can be driven by the shared write-control transistor and the resistance value of write current path is small, the gate width of a write-control transistor in each configuration cell $\left(W_{C}\right)$ can be small.

Figure 3 (a) shows a block diagram for dynamic reconfiguration where a BL driver and four WL drivers are used. If $\mathrm{PG}_{0}$ and EN become high, data ' 0 ' is stored in each configuration cell in accordance with external configuration inputs ( $\mathrm{D}_{1}, \mathrm{D}_{2}$, $\mathrm{D}_{3}, \mathrm{D}_{4}$ ). Similarly, ' 1 ' is stored in each cell when $\mathrm{PG}_{1}$ and EN become high. Figure 3 (b) shows an example of circuit reconfiguration where $\left(D_{1}, D_{2}, D_{3}, D_{4}\right)=(1,0,0,0)$. First, $\mathrm{WL}_{1}$ and BL become high and write current is applied to the Cell1 and ' 1 ' is stored into $\mathrm{Y}_{1}$. Then, $\mathrm{WL}_{2}, \mathrm{WL}_{3}, \mathrm{WL}_{4}$, and BL' become high and write current is applied to Cell2, Cell3, and Cell4, respectively, and $\mathrm{Y}_{2}, \mathrm{Y}_{3}, \mathrm{Y}_{4}$ become ' 0 .' Note that both BL drivers and WL drivers can be shared among several NVLEs.

## 3. Evaluations

For the evaluation, a 6-input NVLE which includes 64 configuration cells is designed using $90-\mathrm{nm}$ CMOS/MTJ technologies. Fig. 4 (a) shows the relationship between the number of configuration cells and write current $I_{W R}$ per cell with 1.2 V strandard supply voltage. The gate width of each configuration cell $\left(W_{C}\right)$ is $2 W_{M I N}$ and that of the shared write-control transistor $\left(W_{S}\right)$ is $40 W_{M I N}$, respectively, where $W_{M I N}$ is the minimum gate width of an NMOS transistor. Even if $I_{W R}$ is decreased to about 0.11 mA when the number of configuration cells is 64 , it is sufficient to program these 64 MTJ devices in 2-ns [5]. Note that the configuration time can be decreased if $I_{W R}$ per cell is increased by dividing the configuration cells into several equal parts together with shared write-control transistors.
Figure 5 shows simulated waveforms of the 6 -input NVLE at 500 MHz using an SPICE macro model [7]. As shown in Fig. 5 (a), AND function is programmed in the first configuration and NAND function is also programmed in the second configuration, respectively. We can also confirm that a correct output level $V_{Z}$ is obtained in accordance with the logic inputs ( $V_{X 1}, V_{X 2}, \ldots, V_{X 6}$ ) as shown in Fig. 5 (b).
Table 1 summarizes comparison of four 6-input NVLEs; a CMOS-based one using 2T-MTJ-based nonvolatile SRAM cells [8], a differential-pair-based one using STT-MTJ devices [3], a differential-pair-based one using a DW shift register [4], and the proposed one. The number of configuration cycles of each STT-MTJ-based NVLE is large since write current must be applied via high MTJ resistance and their configuration cells must be programmed in serial. In the DW-shift-register-based NVLE, the number of write-control transistor is greatly reduced, while large number of cycles are also
required for shifting data. In contrast, the proposed NVLE demonstrates the fastest bit-parallel reconfiguration capability with the smallest transistor counts.

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Figure 1: 3T-MTJ device: (a) Device structure. (b) Symbol.


Figure 2: Proposed 2-input NVLE: (a) Block diagram. (b) 3T-MTJ configuration array.

(b)

Figure 3: Dynamic reconfiguration scheme: (a) Block diagram. (b) Example of reconfiguration (2-input AND function).


Figure 4: Relationship between the number of configuration cells in a parallel write-current path and $I_{W R}$ per cell.

|  | 1st Configuration $\mathrm{PG}_{1}=1 \quad \mathrm{PG}_{0}=1$ | 6-input AND Function | 2nd Configuration $\mathrm{PG}_{1}=1 \quad \mathrm{PG}_{0}=1$ | 6-input NAND Function |
| :---: | :---: | :---: | :---: | :---: |
| $Y_{1}$ |  | '1] |  | '0' |
| $\mathrm{Y}_{2}$ |  | '0' | - | (1) |
| $\mathrm{Y}_{3}$ |  | '0' |  | '1] |
| - | $\xrightarrow[2 n s]{2 n s}$ |  | $\xrightarrow[2 \mathrm{~ns}]{\xrightarrow[2 n s]{ }}$ |  |
| $Y_{61}$ |  | '0' |  | '1] |
| $Y_{62}$ | ${ }_{0}^{1}$ | '0' | - | 4) |
| $Y_{63}$ |  | '0' |  | ${ }^{1}$ |
| $Y_{64}$ | ${ }_{0}^{1} \square$ | '0' | - | '1] |
|  | 0 | 8 |  12 <br> Time [nsec]  <br>   <br>   | 20 |

(a)

(b)

> 90-nm CMOS/MTJ Technologies

Figure 5: Waveforms of the proposed 6-input NVLE:
(a) Stored inputs (partial). (b) Logic inputs and logic output.

Table 1: Performance comparisons.

|  | CMOSBased [8] | Differential-Pair-Based [3] | Differential- <br> Pair-Based [4] | Proposed |
| :---: | :---: | :---: | :---: | :---: |
| Storage | 2T-MTJ Device (STT) |  | 3T-MTJ Device (DWM) |  |
| $\left(R_{P}, R_{A P}\right)^{\left({ }^{(1)}\right)}$ | ( $4 \mathrm{k} \Omega, 9 \mathrm{k} \Omega$ ) |  | $(6 \mathrm{k} \Omega, 24 \mathrm{k} \Omega)$ |  |
| $\left.\begin{array}{\|c\|} \hline \text { Transistor } \\ \text { Counts } \\ \text { (of MTJ.Write. } \\ \text { Control-Transistors } \end{array}\right]$ | $\begin{gathered} 667 \text { Tr. } \\ \text { (128 Tr.) } \end{gathered}$ | $\begin{aligned} & 270 \mathrm{Tr} \text {. } \\ & \text { (70 Tr.) } \end{aligned}$ | $\begin{aligned} & 312 \mathrm{Tr} . \\ & \text { (4 Tr.) } \end{aligned}$ | $226 \mathrm{Tr} .$ |
| Delay ( ${ }^{(2)}$ | 173 ps | 177 ps | 153 ps | 255 ps |
| Active Power @1GHz (*2, 3) | $36 \mu \mathrm{~W}$ | $28 \mu \mathrm{~W}$ | $31 \mu \mathrm{~W}$ | $28 \mu \mathrm{~W}$ |
| \# of Cycles for Configuration | $66{ }^{(4)}$ | 64 | $64\left({ }^{(5)}\right.$ | 2 |

(*1) Estimation from measurement results [9, 10].
(*2) 90 nm CMOS/MTJ technologies ( $V_{D D}=1.2 \mathrm{~V}$ ).
(*3) Average power for logic operation (SEL = 1).
(*4) Two cycles for SRAM configuration and 64 cycles for MTJ one [8].
(*5) Data must be configured using DW shift register [4].

