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Comparative Study of Schottky Barrier Germanium Nanowire Transistors Modulated with Dopant-Segregated Regions

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Abstract

***P*-type Schottky barrier source/drain Ge-nanowire transistors modulated with dopant segregated regions is proposed and studied. The device's performance is simulated with numerical tools. It is revealed that partial depletion of dopant segregated regions is required to increase drive current and reduce leakage current. We also find that the subthreshold slopes of such devices are insensitive to source/drain barrier heights, and we can even obtain lower subthreshold slopes as channel length is scaled down.**

1. Introduction

Recently, Germanium-nanowire has been regarded as an attractive alternative to silicon for devices' channel material, due to its high carrier mobility and gate control ability. After that, Schottky source/drain (S/D) structure is proposed for Ge-based devices, because of the low temperature fabrication requirement. Dopant segregation (DS) technique can feasibly modulate the Schottky barrier height (SBH) and immunize the leakage current. Computational studies of DS Si-based devices have been reported[1-3], and there are few studies on DS Ge-based devices reported, especially on nanowire transistors (NWTs). Herein, we focus on DS-Ge-NWTs for their better performance modulation. The typical *p*-type DS-Ge-NWTs is numerically studied by Sentaurus device simulator, and the effect of DS technique on device performance is studied.

2. Device structure and simulation parameters

The sketches of DS-Ge-NWT are shown in *Fig*.1. The default gate length, L_g=22nm and the nanowire radius, R=5nm. The gate dielectric thickness, T_{ox}=1nm, and gate workfunction engineering is applied to obtain suitable voltage bias. The drain voltage, V_{dd}=-0.5V. There are two kinds of germanide material, PtGe (0.1eV for holes[4]) and NiGe (0.18eV for holes[5]), used at S/D sides for comparisons. The structure is set with undoped channel and heavily doped DS regions. The dopant concentration in DS region, N_{seg}, varies from 10^{19} to 10^{21}cm^{-3}, with 10^{20}cm^{-3} as default; and the length of DS region, L_{seg}, varies from 1 to 8nm, with 3nm as default. The applied models and tunneling mass of Ge is calibrated with the experimental results of Ge-based *p*-type planar SB-MOSFET[6].

3. Results and discussion

Fig.2 shows the 2D potential distributions along SB-Ge-NWT's (without DS regions) and DS-Ge-NWT's channel regions. We can find that DS-Ge-NWT has higher potential change rate at source side and thicker Schottky barrier region at drain side. *Fig*.3 plots the hole current density distributions along the two devices'channel regions. DS-Ge-NWT can achieve larger current at source side because of the large hole tunneling probability, induced by highly doped DS region. *Fig*.4 displays the transfer curves of SB-Si-NWT, SB-Ge-NWT, and DS-Ge-NWT. We can find DS-Ge-NWT has both high ON-state current and low subthreshold swing (*SS*).

Fig.5 plots the I_{on}-N_{seg} curves of DS-Ge-NWTs with different SBHs at S/D contacts. It is found I_{on} keeps constant for low N_{seg} and increases sharply at a certain point. It can be explained that partially depleted DS regions, resulted by high dopant concentration, is demanded to reduce SB thickness effectively for large tunneling current[2]. Another notable phenomenon is that high SBH, which means a thick SB, requires large N_{seg} to be partially depleted.

In *Fig*.6, the relation between the minimum OFF-state current, I_{min}, and N_{seg} is plotted. I_{min} decreases as N_{seg} increases for SBH=0.1eV, while there is a turning point for other SBHs, which is consistent with the work for silicon[2]. *Fig*.7 displays the 2D potential distributions at I_{ds}=I_{min} with N_{seg}=10^{19}cm^{-3} for SBH=0.1eV and 0.18eV, respectively. For SBH=0.18eV, we can deduce that I_{min} is mainly influenced by the increment of hole current, until the thick SB at drain side caused by partial depletion makes the decrease of electron current the domain factor. For SBH=0.1eV, electron current plays a main role in constituting I_{min} for the whole range of N_{seg} investigated. Another result plotted in *Fig*.8 indicates that *SS* has a similar tendency as I_{min} when N_{seg} changes from 10^{19} to 10^{20}cm^{-3}.

Fig.9 plots I_{on}-L_{seg} curves with different SBHs for N_{seg}=10^{19} and 10^{20}cm^{-3}, respectively. For N_{seg}= 10^{19}cm^{-3}, I_{on} changes a little when L_{seg}>4nm, while N_{seg}=10^{20}cm^{-3}, there is a turning point at L_{seg}=4nm. *Fig*.10 explains this result by plotting the hole density distributions with L_{seg}=2nm, 4nm, and 6nm, respectively. It is shown that long L_{seg} leads to accumulation at S/D sides, thus reducing hole current.

Fig.11 shows the relation between *SS* and SBH. We can find that *SS* of SB-Ge-NWT increases as SBH increases, and *SS* of DS-Ge-NWT with L_{seg}>3nm is insensitive to SBH. The relationship between *SS* and L_{seg} is plotted in *Fig*.12. We can see that DS-Ge-NWT has lower *SS* than SB-Ge-NWT and DS-Ge-NWT with longer L_{seg} has larger *SS* due to the decrease of effective L_g. When L_g is reduced to 12nm, this effect becomes so severe that DS-Ge-NWTs with L_{seg}=3 and 4nm have the same *SS* as SB-Ge-NWT's.

4. Conclusion

In this paper, we have simulated and analyzed the characteristics of DS-Ge-NWT by a TCAD modeling method. It is confirmed that in DS-Ge-NWT, a thin SB at source side is created by DS region, which brings high I_{on} and better *SS*. It is also noticed that partial depletion in DS regions is required to get large drain current and suppressed I_{min}. Interesting phenomena observed in I_{min}-N_{seg} curves and I_{on}-L_{seg} curves are discussed by analyzing electrical properties of device performance. Moreover, *SS* of DS-Ge-NWT is insensitive to SBH, and DS-Ge-NWT has lower *SS* when L_g is scaled down.

Acknowledgement

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Reference

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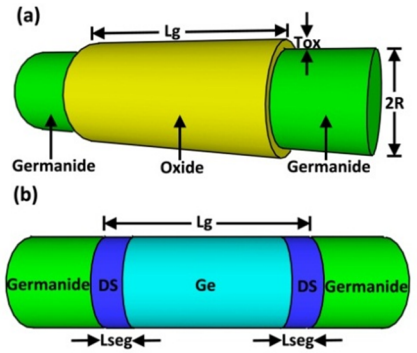

Fig.1. Sketches of (a) DS-Ge-NWT with gate oxide and (b) without gate oxide.

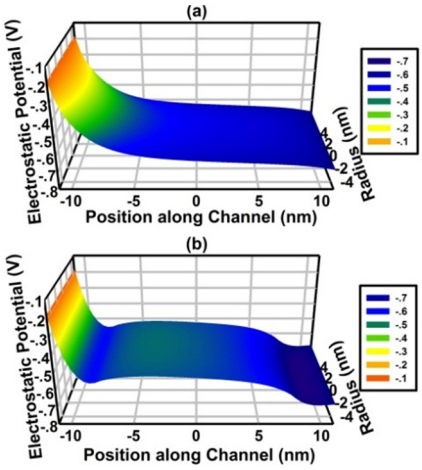

Fig.2. 2D Potential distribution along channel: (a) SB-Ge-NWT and (b) DS-Ge-NWT.

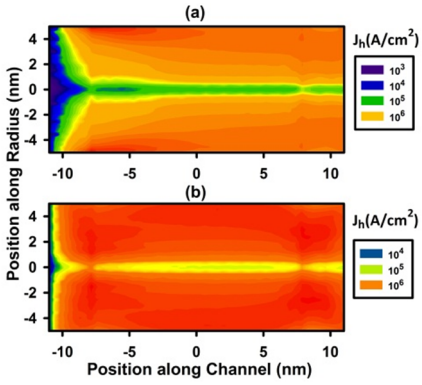

Fig.3. Hole current density distribution along channel: (a) SB-Ge-NWT and (b) DS-Ge-NWT.

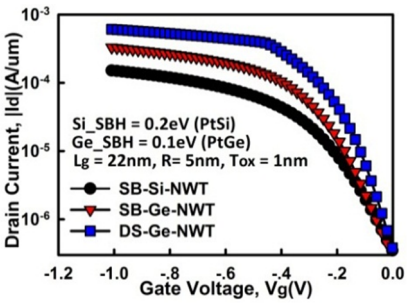

Fig.4. Transfer curves of SB-Si-NWT, SB-Ge-NWT, and DS-Ge-NWT.

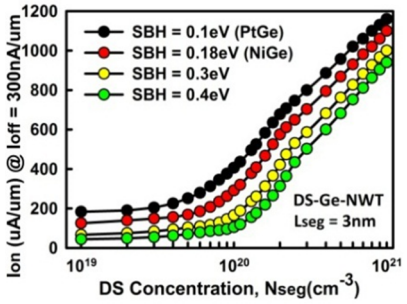

Fig.5. I_{on} versus N_{seg} with multiple SBHs.

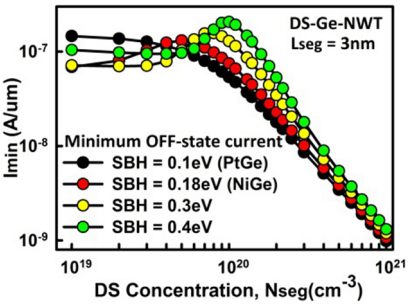

Fig.6. I_{min} versus N_{seg} with multiple SBHs.

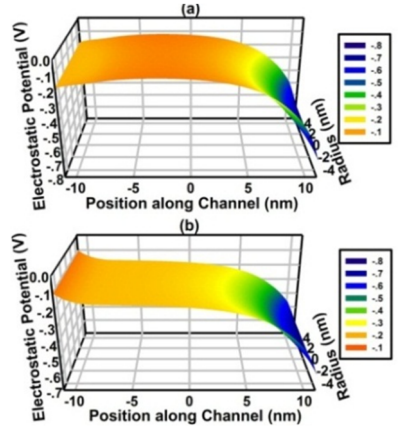

Fig.7. 2D Potential distributions at I_{ds}=I_{min} for (a) SBH=0.1eV and (b) SBH=0.18eV.

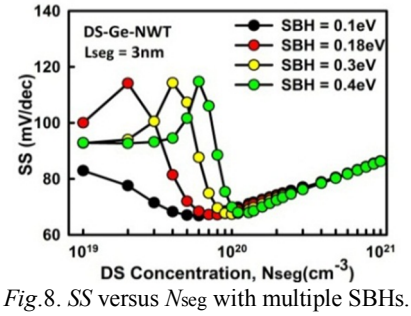

Fig.8. *SS* versus N_{seg} with multiple SBHs.

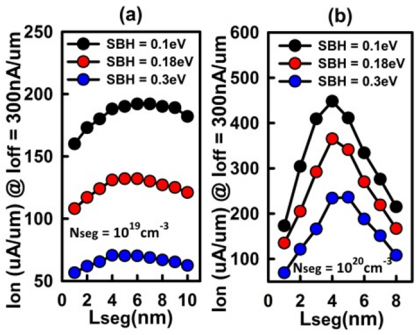

Fig.9. I_{on} versus L_{seg} with (a) N_{seg} =10^{19}cm^{-3} and (b) N_{seg}=10^{20}cm^{-3}.

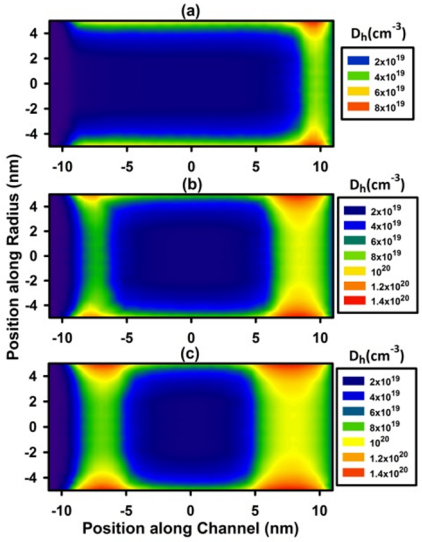

Fig.10. Hole density distributions with L_{seg} equals: (a) 2nm, (b) 4nm and (c) 6nm. N_{seg}=10^{20}cm^{-3}.

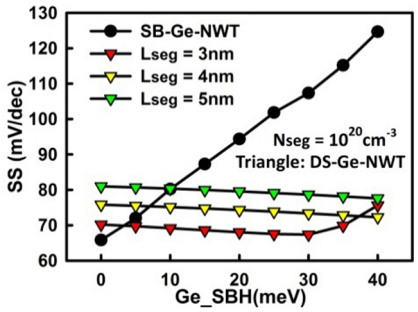

Fig.11. *SS*-SBH curves of SB-Ge-NWT and DS-Ge-NWT with different L_{seg}.

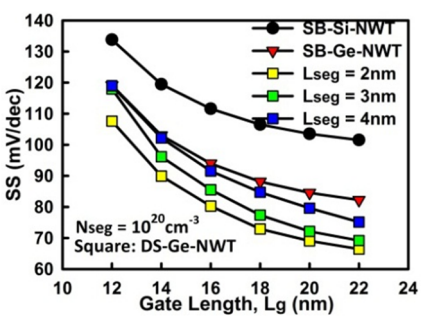

Fig.12. *SS*-L_g curves of SB-Si-NWT, SB-Ge-NWT and DS-Ge-NWT.