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Investigation of Via Degradation Behavior under Thermal Cycling Stress on Power Device

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Abstract

This paper describes via degradation behavior under thermal cycling stress on power device. The via resistance increased gradually under thermal cycling stress, and finally disconnected after millions of cycles. Via failure time under thermal cycling stress is shorter than under DC thermal stress. The failed via broke into two parts, with the top half being partly driven into the top aluminum line, and bottom half being driven into the bottom aluminum line. These results demonstrate that the degradation mechanism can be attributed to the repetition of expansion and contraction in the via and aluminum lines due to the thermal cycling stress, so-called thermo-mechanical stress. We have proofed that the cycles to failure depends on the temperature rise in the thermal cycling stress.

1. Introduction

Power device, e.g. DMOS transistors are widely used in automotive applications as low-side switches driving inductive loads (Fig.1). Thermal cycling is generated by power dissipation when the DMOS switch is in operation. It results the thermo-mechanical stress, which causes failure like interlayer dielectric crack. [1~2] Therefore, evaluating the reliability of the DMOS device under thermal cycling stress is very important. When we evaluated the DMOS device under thermal cycling stress, we found out that via degraded gradually and disconnected after millions of cycles. This via degradation behavior has never been reported, and so is worthy of being investigated in detail.

2. General Instructions

The test structure consisted of a heater, bottom aluminum line, via, top aluminum line and interlayer dielectric (Fig.2). It was fabricated in a 0.25μm BCD process. The via was filled with tungsten, and the size was 0.3μm. The aluminum line width is 14μm. The heater was formed from poly silicon instead of DMOS device. It was designed meander shape in order to provide an effective temperature rise. The heater generated thermal cycling stress, or DC thermal stress, by inputting repetitive pulse or DC voltage. Via resistance was measured by running a current from the top aluminum line to the bottom aluminum line. Fig.3 shows the schematic of the measurement setup. The evaluation of via degradation was performed on wafer-level. A semiconductor parameter analyzer supplied the repetitive pulse or DC voltage to the heater and measured via resistance as the same time by using sampling mode. To test the operation of the test structure, the resistors R1 and R2 were inserted in the low side of the heater and via, respectively. Fig.4 shows, that the VR1 changed periodically due to the repetitive pulse inputted to the heater. The period and width of the pulse was 10ms and 8ms, respectively. How-

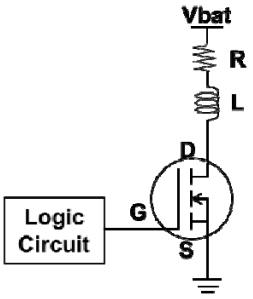

Fig. 1 Circuit diagram of a low-side switch driving an inductive load.

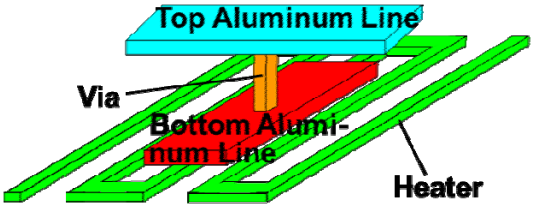

Fig. 2 Image of the test structure.

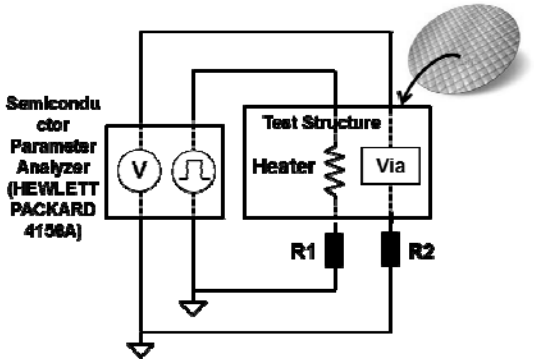

Fig. 3 Schematic of the measurement setup.

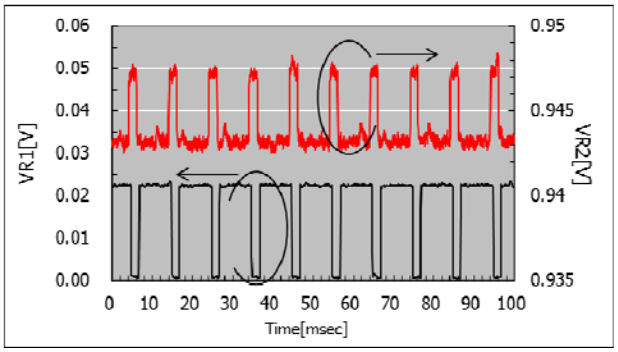

Fig. 4 Voltage change of R1 and R2 while repetitive pulse is inputted to the heater.

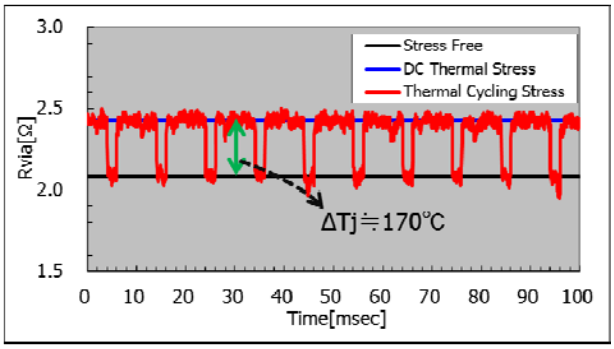

Fig. 5 Via resistance change under thermal cycling stress (Vpeak=15V) and DC thermal stress (Vdc=15V).

ever, the VR2 changed inversely to VR1. It was confirmed that the via resistance increased because of the temperature rise due to the thermal cycling. Fig.5 shows the via resistance measured under thermal cycling stress (Vpeak=15V) and DC thermal stress (Vdc=15V). The resistance change was same in both stress conditions, which indicates the temperature rise ΔTj was the same, and the ΔTj was estimated to reach up to 170℃. Fig.6 shows the via resistance change over time under DC thermal stress and thermal-cycling stress. The resistance change under DC thermal stress (attributed to electromigration) was only 1% after 72hrs. In contrast, under thermal cycling stress, it took only 2hrs to reach the same degradation level. A significant

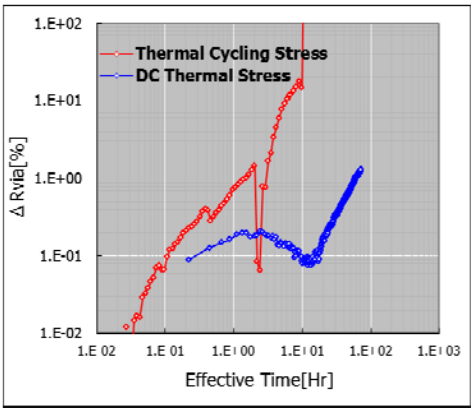

Fig. 6 Via resistance change over time under thermal cycling and DC thermal stress with same temperature rise of 170℃.

difference in failure time between thermal cycling stress and DC thermal stress was confirmed. Therefore, the via degradation was mainly due to thermal cycling stress. Fig.7 shows a TEM cross sectional view of a failed via. The via was broken into two parts, with the top half being partly driven into the top aluminum line, and bottom half being driven into the bottom aluminum line. This suggests that the main cause of the failure mechanism was the contraction and expansion (thermo-mechanical stress) due to thermal-cycling. Fig.8 shows the temperature rise dependence of cycles to failure. The criterion is via resistance change with 5%. It suggests that the cycle to failure depends on the temperature rise.

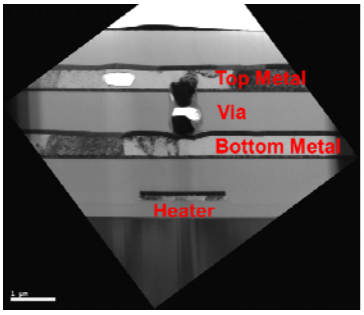

Fig. 7 SEM cross sectional view of a deformed via after millions cycles.

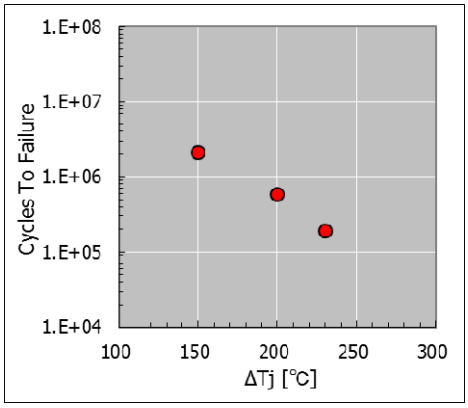

Fig. 8 Temperature rise dependence of cycles to failure. (Ta=RT)

3. Conclusion

The via degradation behavior under thermal cycling stress on power device was investigated. We proofed the via degradation mechanism can be attributed to the repetition of expansion and contraction in the via and aluminum lines due to the thermal cycling stress, so-called thermo-mechanical stress.

References

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[2] Chris Kendrick et al.,"Reliability of NLDMOS Transistors Subjected to Repetitive Power Pulses", IRPS, 2008, pp. 651-652