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Evaluating the cryogenic performance of SiC PiN diodes.

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Abstract

Extensive high-resolution cryogenic performance testing is carried out on 4H-SiC PiN diodes. At 2K intervals from 20 to 320K, current-voltage, and capacitance-voltage tests are performed to extract turn-on, ideality factor, carrier density, reverse leakage and barrier height data across the temperature range. We also analyse the switching performance of the diodes across the same temperature range using an inductive switching setup.

1. Introduction

The wide bandgap, high critical electric field and thermal conductivity of SiC has placed the material at the forefront of power electronics research. High defect densities have mostly confined SiC device production to fast switching unipolar devices such as Schottky diodes, MOSFETs and JFETs, while the current rating of these devices is restricted by the continued presence of killer defects, limiting device area. Even SiC BJTs exploit low carrier lifetimes to bias their devices towards fast switching rather than the low conduction losses that would enable high voltage (10kV+) power devices. However, as the materials quality has improved [1], micropipe free wafers have become available [2] and the density of non-killer defects such as basal-plane dislocations have dropped to new lows [1,3], making possible a new generation of high voltage bipolar device such as the SiC IGBT and thyristor.

In this work, we study the cryogenic performance of SiC PiN diodes carrying out current-voltage-temperature (IVT), capacitance-voltage-temperature (CVT) and switching performance tests at temperatures between 20 and 320 K, with a resolution of up to 2 K. The main motivation for low temperature power electronics comes from potential space applications [4] and increasingly, the need for the co-location of control electronics next to a high-current superconducting device in, for example, the field winding of a synchronous machine [5,6].

Carrier freeze-out occurs in a semiconductor when the carrier density drops below the intended doping level. The cryogenic testing of SiC diodes is therefore of scientific interest when compared to say Si PiN diodes [7], because the extra energy require to cross the wide bandgap of SiC means that carrier freeze-out occurs at much higher temperatures than it does in Si. Hence, it is much easier to study the effects of carrier freeze-out on all aspects of the PiN diode response.

2. Experimental Processes

The PiN diodes used in this work were fabricated in-house from a 3-inch *n*-type (0001) Si face, 4° off axis, <1 micropipe/cm^2 4H-SiC wafer purchased from Dow Corning with a 30 µm, lightly *n*-type doped (2x10^{15} cm^{-3}), epitaxial layer, and a 250 nm, highly *p*-type doped (>1x10^{19} cm^{-3}) grown in a continuous growth run at Norstel. After epitaxial growth, the material has been laser-cut into 14x14 mm dies. Once cleaned and individual anodes mesa-isolated, ohmic contacts were formed to the front (Ti/Al/NiV) and backside (Ti/NiV) and were rapid thermal annealed at 1000C for 2 minutes. The devices were characterised using a fully automated closed-cycle-cryostat test setup, which allowed current-voltage measurements to be taken between 20 and 320 K at 2 K intervals.

3. Results and Discussion

The full set of forward characteristics are shown in Figure 1, the shape of which is formed by competing temperature dependencies [7]. As the temperature drops, so the carrier density drops, widening the energy gap between the *n*- and *p* doped regions. This causes the shift in voltage shown in Figure 1, each step lower in temperature, requiring more voltage either to overcome the potential barrier (in thermionic emission) or for recombination to occur. However, as seen in Figure 2, the carrier concentration drops dramatically below 75 K. This has the effect of dramatically increasing the bulk mobility, and hence lowering the device's resistance. Therefore, the turn-on voltage, when considered at the more practical, higher current level of 1A/cm^2 as shown in Figure 2 will dramatically reduce below 75 K.

Figure 3 shows the ideality factor (η), as it varies against both temperature and voltage. The ideality factor profile was found by differentiating the current-voltage profile and comparing the result to the empirical form [8] of the current-voltage relationship, $J_F \propto \exp(qV/\eta kT)$. Figure 3 shows that the devices begin to turn on at low current levels with recombination dominating, as $\eta \geq 2$. η then drops to a minima of around 1.2 as thermionic emission becomes dominant, before series resistance takes hold. The minima relates only to the point at which series resistance begins to impose, and hence the faint positive correlation between this minima and voltage is related to the increasing series resistance as temperature increases. At 320 K, the ideality factor reaches a minimum of 1.27, at which point the barrier height – referring to the conduction/valence band offset – can be equated from the thermionic emission equation [8], as 2.62 eV. A subset of reverse characteristics is shown in Figure 4, showing the reverse leakage currents increasing with temperature at a reverse bias of 100 V.

In the final submission, the results already presented will be accompanied with further analysis using two other techniques. C-V-T analysis will be used to will confirm our doping profiles, and to confirm the modelling of the carrier density profile shown in Figure 2. We shall also include switching tests across the temperature range using an inductive switching setup connected to the closed cycle cryostat. This will show the extent to which switching characteristics such as reverse recovery improve at cryogenic temperatures, as they do within Si PiN diodes [7].

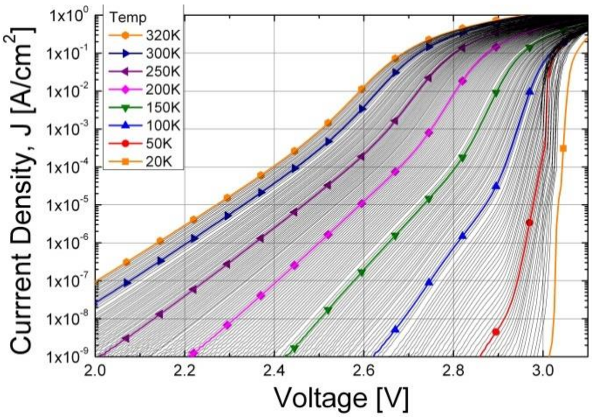

Fig. 1: J-V characteristics of the SiC PiN diode measured at 2K intervals from 20 to 320 K.

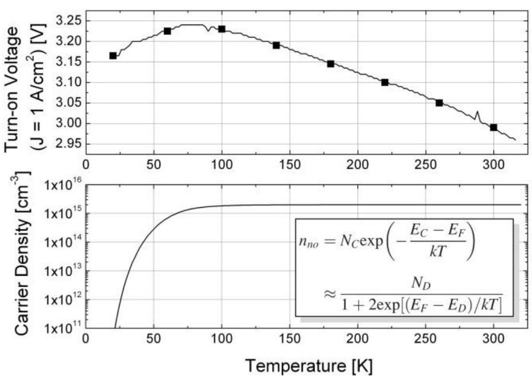

Fig. 2: Top: The PiN diode turn-on voltage (at 1 A/cm^2) plotted against temperature. Bottom: the current density profile modelled using the equations in the inset, from [8].

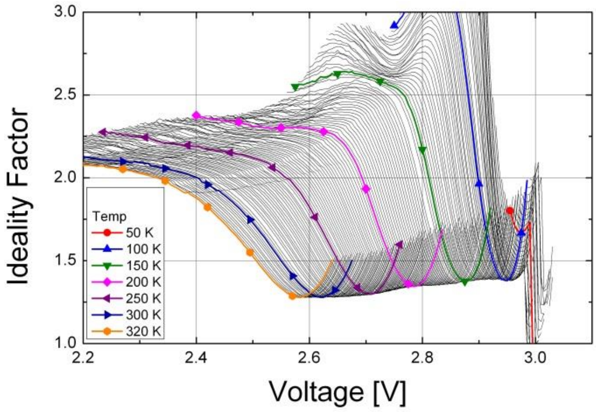

Fig. 3: The ideality factor of the PiN diode responses varying with temperature and with voltage.

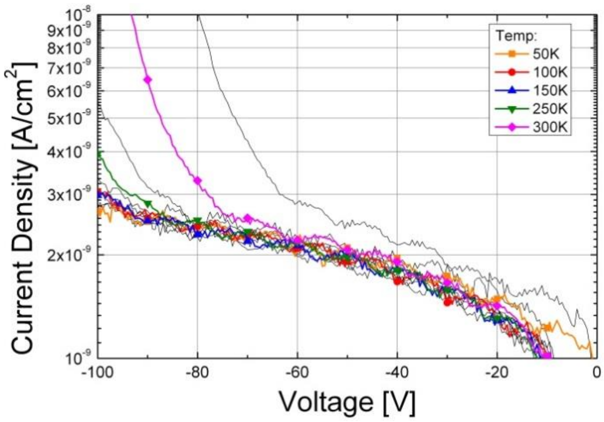

Fig. 4: The reverse leakage of the SiC PiN diode measured at 10 K intervals from 20 to 320 K.

Acknowledgements

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