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Cell Pitch Design Limitation for Electrical and Thermal Characteristics in Super Junction MOSFET

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Abstract

In Super Junction (SJ) MOSFET, Cell pitch parameter has to be considered because of the on-resistance characteristics. Unlike conventional Power MOSFET, SJ MOSFET has opposite tendency of the on-resistance characteristics when cell pitch is reduced. In this paper, electrical and thermal characteristic effects of the cell pitch degradation in SJ MOSFET are simulated to confirm opposite tendency using TCAD tool.

1. Introduction

The most important issue for semiconductor power devices is reducing the conduction loss that occurs when it turned on[1-3]. SJ MOSFET has far superior electrical characteristics, such as higher voltage and lower on-resistance, to those of conventional high-voltage MOSFETs[7]. The power electronics market is demanding low on-resistance at an appropriate voltage level. So on-resistance is the most important parameter when SJ MOSFET is designed. In conventional Power MOSFET, reducing cell pitch parameter has been used to decrease on-resistance[8]. But in SJ MOSFET, reducing cell pitch makes on-resistance increases because device current path area is decreasing with steady value of on-state depletion layer width[9]. Additionally, reducing cell pitch results in a higher breakdown voltage and thermal resistivity. In this paper, cell pitch limitation is proposed using relationship of cell pitch, electrical and thermal characteristics confirmed by TCAD simulation.

2. Result

2.1 Basic analysis

On-resistance analysis in SJ MOSFET differs from conventional MOSFET due to P pillar structure. Reducing cell pitch, n pillar width is almost same with that of non-reducing cell pitch. That result can be assumed in eq.(1)[9].

$$R_{on} = \rho_D L_D \left(\frac{W_{Cell}}{W_N - W_{Depletion-N}} \right) \qquad (1)$$

W_{Cell} means full cell width of SJ device, W_N is the n pillar width and $W_{Depletion-N}$ is the depletion width of on-state drain voltage biased in the N, P pillar junction area. Because the $W_{Depletion-N}$ parameter is related in forward bias drain-source voltage, $W_{Depletion-N}$ is constant when cell pitch is decreasing. So Ron is increasing with both W_{Cell} and W_N reduced due to uniform $W_{Depletion-N.}$ It can be observed in Fig.1.

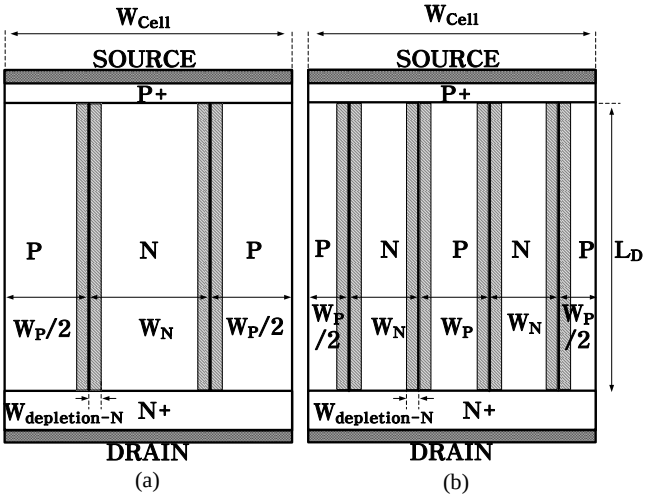

Fig. 1 Relationship of cell pitch decreasing and depletion width. (a) N pillar path = W_N-2$W_{Depletion-N}$. (b) N pillar path = W_N-4$W_{Depletion-N}$

In Fig.1, (b) structure has half of the cell pitch compared with that of (a). But W_{DN} of (b) structure is 2 times larger than that of (a). So reducing cell pitch is affected on on-resistance characteristics degradation in SJ MOSFET.

Cell pitch modulation also affects thermal resistivity.

When current path is decreasing, the same current is flowing in narrower area than that of wider one. So in narrower cell pitch, Thermal resistivity is larger than wider one.

2.2 Simulation result

In order to study the cell pitch limit according to the electrical and thermal characteristics, the SJ MOSFET structure for 600V is simulated. The doping concentration of the N, P pillar is $4.73 \cdot 10^{15} cm^{-3}$ and $5.93 \cdot 10^{15} cm^{-3}$. Drift depth is 59μm and 9, 13, 17, 21μm cell pitch are simulated. As shown in Fig.2, on-resistance is rapidly increasing at 13 μm cell pitch and also increasing breakdown voltage in trade-off relation when cell pitch is reduced. To achieve best breakdown voltage characteristic, cell pitch has to be decreasing. But on-resistance in SJ MOFET is more drastically increasing compared with the breakdown voltage about two times. So cell pitch limitation is needed to achieve best on-resistance characteristics. Optimum point of cell pitch is 13 μm at relation of breakdown voltage versus on-resistance in Fig.2.

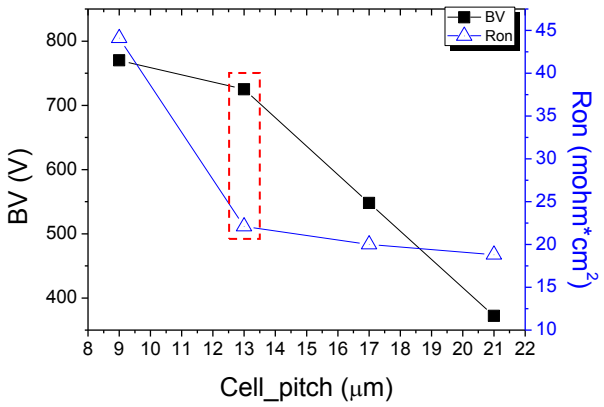

Fig. 2 Breakdown voltage and on on-resistance characteristics of cell pitch modulation.

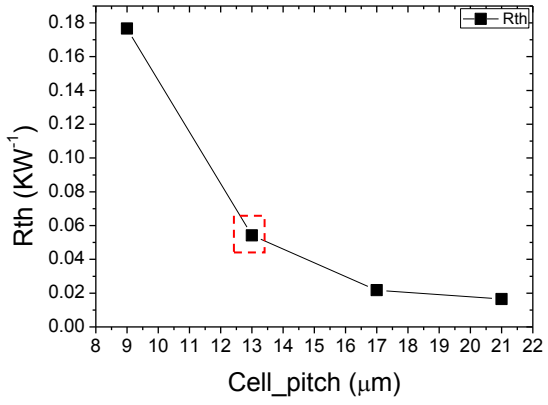

Fig. 3 Thermal resistance characteristics of cell pitch modulation.

This cell pitch limitation also is needed in Thermal resistance characteristic. As shown in Fig.3, Thermal resistivity is rapidly increasing with cell pitch shrinking. This simulation is based on same area and current, $1cm^2$ and 100A. When cell pitch is reducing, cross sectional area of current path is decreasing and heat generation is also increasing. So higher T_1-T_2 is achieved and R_{th} is abruptly increasing. Cell pitch limitation has to be needed in thermal characteristics by high thermal resistance, R_{th}. 13 μm cell pitch is optimum point of heat characteristics as shown in Fig.3.

3. Conclusions

Conventional Power MOSFET can have low on-resistance characteristic using cell pitch reducing. But in SJ MOSFET, reducing cell pitch cause increasing of on-resistance due to decreasing of N pillar width with uniform on-state depletion width. And cell pitch degradation cause increasing of thermal resistivity too. So Cell pitch limitation has to be needed. In this paper, 600V SJ MOSFET has optimum point of 13 μm cell pitch. This cell pitch limitation can apply with other voltage size devices in further paper issues.

Acknowledgements

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