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Hot carrier effect of a scaled thin-film SOI power MOSFET under constant drain electric field

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Abstract

This paper describes the hot carrier effect of the thin-film SOI power MOSFET with shrinking the design rule. The device degradation caused by hot carrier effect is promoted by shrinking the design rule despite the shrinking under constant drain electric field.

1. Introduction

Power ICs fabricate using SOI technology have become attractive because they can completely isolate the devices each other and can operate high temperature[1]. A thin-film approach has been quite promising because it can not only easily isolate devices from each other but can also combine thin film CMO/SOI devices without deep diffusion process usually needed for power devices[2].

The one of the most important concern related to the thin-film SOI power MOSFET(Fig. 1) is how to improve their high-frequency switching performance. This have been actively studied by reducing the on-resistance and parasitic capacitance[3]. The one of the most effective ways to do these is to shrink the channel length with keeping electric field of the drift region. In this case, only the channel length reduces without changing drift length. However, it has not been clarified between shrinking the gate length and device degradation caused by hot carrier effect under constant electric field of drift region.

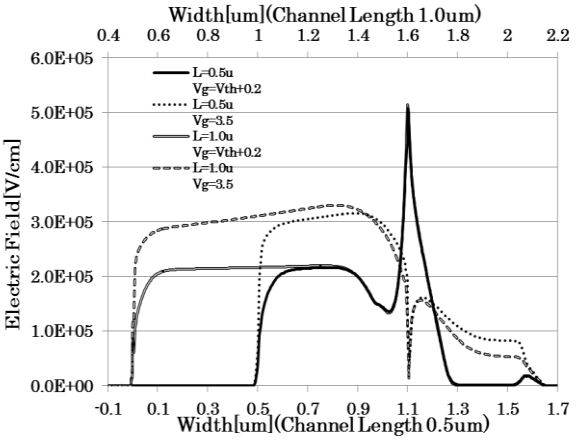

Fig. 1 Comparisons of the Electric field distribution of the thin-film SOI power MOSFETs.

This paper describes the hot carrier effect of the thin-film SOI power MOSFET for scaling the device under constant electric field of drift region.

2. Device structure and Fabrication process.

The schematic cross section of the fabricated thin-film SOI power MOSFET is shown in Fig.2. The body contacts were formed to suppress the parasitic bipolar effect and the main structural parameters are listed in Table 1. The SOI power MOSFET was fabricated using 0.5μm-rule polycide gate process with LOCOS isolation.

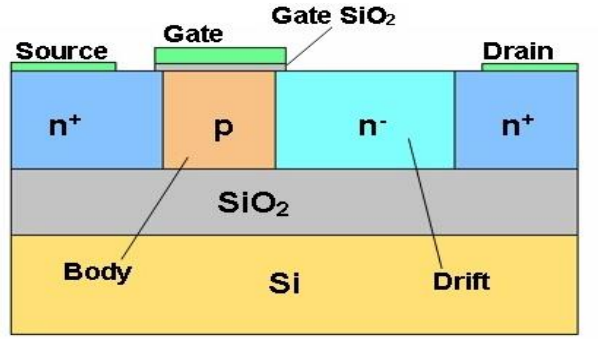

Fig. 2 Schematic cross section of SOI power MOSFET.

Table. 1 The main structural parameters.

Top Si layer(μm)	0.14
Buried oxide(μm)	0.4
Gate oxide(nm)	11
Channel Length(μm)	0.5,1.0
Drift Length(μm)	0.5

Table. 2 Device characteristics

	Channel Length(μm)	
	0.5	1.0
Threshold voltage(V)	0.540	0.550
On-Resistance(Ω)*	625	867
Breakdown voltage(V)	14.0	14.4

*Vg=5.0(V)

Main device characteristics are listed in Table 2. Threshold voltage of the both MOSFETs are almost the

same. On-resistance of the device with smaller channel width is lower. The breakdown voltage is almost the same because the drift length of the both MOSFETS are the same. This means that scaling was performed by keeping the electric field.

3. Result & Discussion

Dependence of threshold voltage shift on the stress gate voltage is shown in Fig. 3. Stress time is 10,000 seconds. Drain voltage is 6V. The threshold voltage shift of the device with channel length of 0.5μm is larger and it increases with increasing the gate stress voltage. On the contrary, threshold voltage shift did not occur in the channel length of 1.0μm

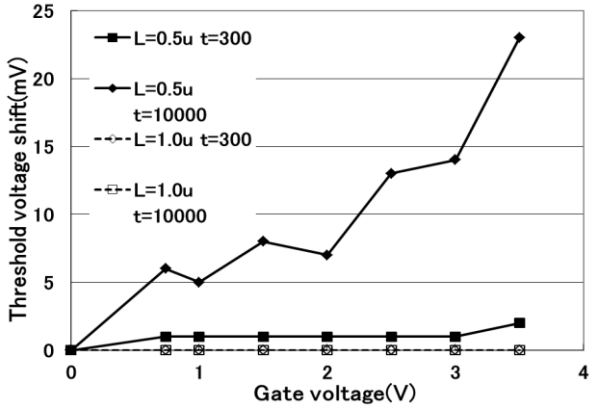

Fig. 3 Dependence of the stress gate voltage on threshold voltage shift.

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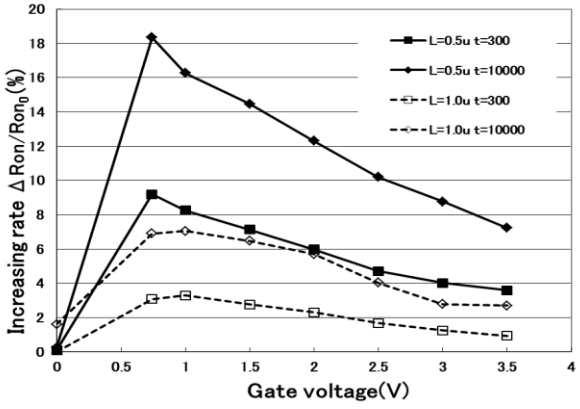

Fig. 4 Dependence of stress gate voltage on the on-resistance degradation rate.

Dependence of degradation rate of on-resistance on stress gate voltage is shown in Fig. 4 and dependence of the degradation rate of on resistance on stress time is Fig.5. The degradation rate of the on resistance shows the maximum value near the threshold ((Vth+0.2)V). The degradation rate of the device with channel length of 0.5 μm is higher than that of 1.0 μm despite the same electric field. Degradation pronounced at an early stage, and it is

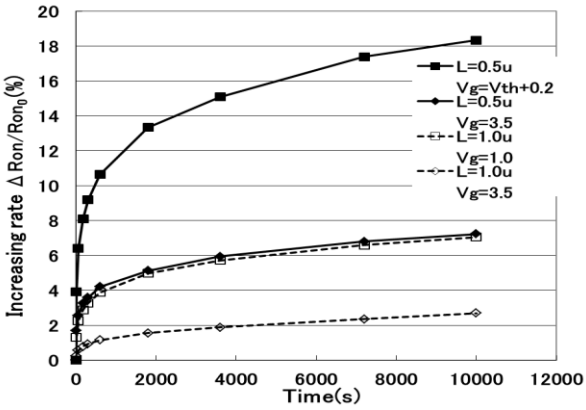

Fig. 5 Dependence of stress time on the on- resistance degradation rate.

saturated[3]. There are two kinds of degradation of on-resistance by hot carrier injection[3]. The one is degradation near threshold voltage. In this case, the high electric field appears near the gate edge of the drain junction. The high electric field induces parasitic bipolar effect and promotes avalanche hot carrier injection[3]. The extension of the depletion lay is enhanced by hot carrier injection and this reduces the electric field. Thus, on -resistance increases. These results indicated that larger degradation in device with smaller channel length is caused by parasitic bipolar effect. The other is degradation at high stress gate voltage. In this case higher electric field appears channel region and channel hot carrier injection is occurred. Channel hot carrier injection decreases mobility and this increases on-resistance.

4. Conclusions

The hot carrier effect of a thin-film SOI power MOSFET has been studied. The threshold voltage shift enhanced by increasing the gate stress voltage. The degradation of the on-resistance is the largest when the gate stress voltage is near threshold. In this case, hot carrier effect was enhanced by parasitic bipolar effect. Device degradation caused by hot carrier effect is always higher for device with smaller channel length even though the same electric field..

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