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Floating Field Plate HV-MOSFET by 28nm High-k Metal Gate Process

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Abstract

Abstract—Strength of surface electric field distribution strongly influences on breakdown voltage and reliability of MOS transistors. This work presents floating field plate (FFP) design for 28nm high-k metal gate MOS transistors. Floating metal gates are employed to extend the corner electric field at edge of drain junction under the thin core gate dielectric layer. The design of floating field plate on potential profiles and surface electric field distributions are studied by simulation data. Measurement results demonstrated that the floating field plates can effectively raise the gated breakdown voltage to the junction limit without process modifications.

Introduction

As technology scales, the maximum voltage circuits can endure generally reduces drastically as a result of aggressive source/drain junction and well engineering to improve the transistor performance levels [1]-[3]. The drain breakdown voltage is typically limited by the gated breakdown, which results from the high electric field at the surface of the drain junction at off-states [4]-[6].The use of the lightly-doped drain (LDD) structure reduces the electric field at this edge, hence increases the drain breakdown voltages[7]-[8]. Drain extended (DE) MOS transistors with a drain extension can operate at much higher drain voltage [9]-[11].The above approaches either require addition processing steps or mask layers. The challenge become greater as CMOS technology's continuous scaling leads to sharper junction and thinner dielectric layer. Field-limiting ring (FLR) and field plate (FP) structures [12]-[13] are commonly used in the junction termination design. In this work, MOS transistor with Floating Field Plate (FFP) to increase breakdown voltage is proposed and demonstrated in advanced nano-meter CMOS technologies.

Device Structure and Characteristics

The inset in Figure 1 shows the TEM of a conventional NMOSFET with a gate length of 90nm prepared by the 28nm CMOS technology. The breakdown characteristics of devices with different length summarized in Figure 1 indicates that gated breakdown voltage cannot be improved by increasing channel length. Furthermore, due to the small Effective Oxide Thickness (EOT~1nm) on these high-k metal gate devices, the gated breakdown of 5V is much worse than what the n+/p-well junction can endure. The proposed FFP MOS transistors are illustrated in Figure 2, where the floating gates (FG) and the n^+ regions acts like as the field plate and field-limiting rings, respectively. As the drain potential is coupled to these FGs, the gated breakdown voltage can be reduced effectively. The geometric parameters for all test samples in this study are listed in Table1. The simulated potential distributions of the FFP MOSFET in its off-state are arranged in Figure 3. As the drain voltage increases ,the floating gates coupled by the drain extends the deletion region to allow more potential drop under the FG region, hence, alleviating the high electric field occurred in this region. The effect of field plates are clearly demonstrated in these plots, where the maximum electric field is effectively reduced, as shown in Figure 4. As expected, the simulated gated breakdown voltage increases to close to n^+/p-well junction breakdown limit when number of FGs exceeds 6 (see Figure 5). Figure6 compares the simulated specific on-resistance ($R_{on\text{-}sp}$) at V_{GS}=1V.Since drain coupling cannot fully turn on the channel under FG, the $R_{on\text{-}sp}$ is expected to decrease. FFP MOSFETs with number of FGs =1,3,6 prepared by 28nm CMOS logic process are demonstrated in the Figure 7. As reveals in these pictures, the FFG structure is well formed with desirable coupling structures. Figure 8 compares the measured breakdown characteristics of these test samples. These results agree with simulated data in Figure 5 that the increase of gated breakdown saturated as the number of FGs increase to above 6. Figure 9 shows the measured drain current characteristics for MOSFET with different number of FGs. $R_{on\text{-}sp}$ degraded substantially when number of FGs increases. FG potential of different FFP MOSFETs under V_D=1V and 3.3V are compared in Figure 10, suggesting that the FFP devices provide better on-state characteristics when driven by a higher drain voltage. Measured specific on-resistance vs. the breakdown voltage of the different FFP MOSFETS is plotted in Figure 11. Data reveals that the FFP device exhibit the best tradeoff between the breakdown voltage and on-resistance with number of FGs between 3 and 4.

Conclusion

In this paper, we present a floating field plate (FFP) MOS transistors realized by 28nm high-k metal gate CMOS technology for high-voltage operation. The improved breakdown voltage can reach the junction limit at around 10V. Number of floating gates should be optimally designed without seriously degrading the on-state characteristics

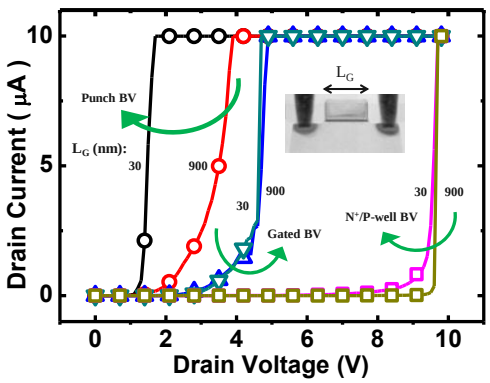

Figure 1 Breakdown characteristics of typical transistor at different length, transistor TEM is shown in the inset.

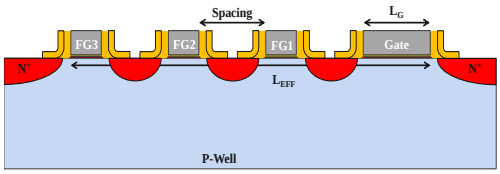

Figure 2 Proposed FFP MOSFET with design parameters of FG spacing and channel length.

Sample	Gate		Floating Gate				
	Length	Width	count	Length	Width	Spacing	L_{EFF}
#1	90nm	120nm	0				90nm
#2	90nm	120nm	1	40nm	120nm	90nm	220nm
#3	90nm	120nm	3	40nm	120nm	90nm	480nm
#4	90nm	120nm	6	40nm	120nm	90nm	870nm
#5	90nm	120nm	9	40nm	120nm	90nm	1260nm

Table1Geometric parameters used for designing the FFP MOSFETs

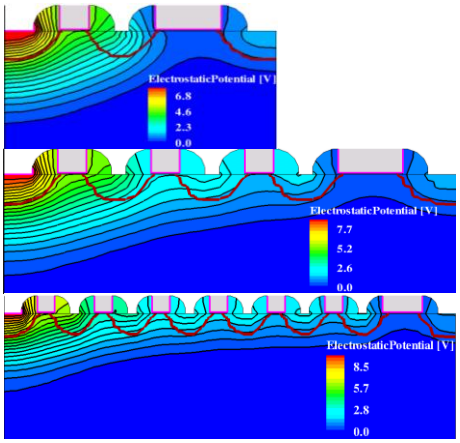

Figure 3 Potential distribution of the FFP MOSFETs with different number of FGs.

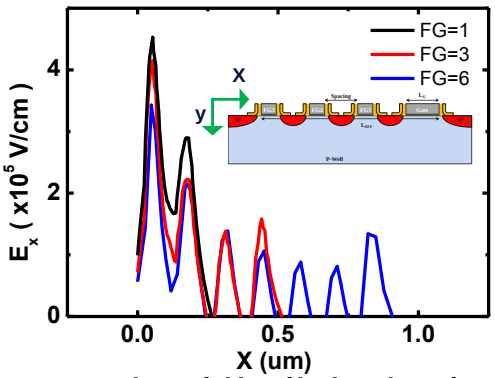

Figure 4 Electric field profile along the surface for different FFT MOSFETs

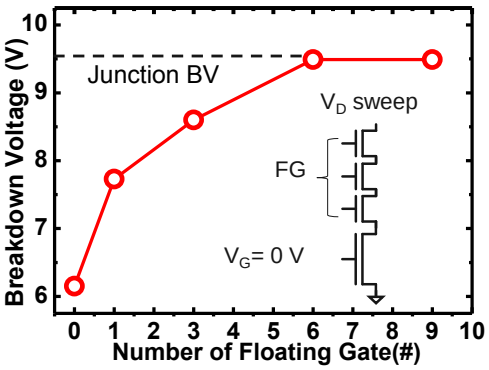

Figure 5 Simulated breakdown voltages of FFP MOSFETs with different number of FGs.

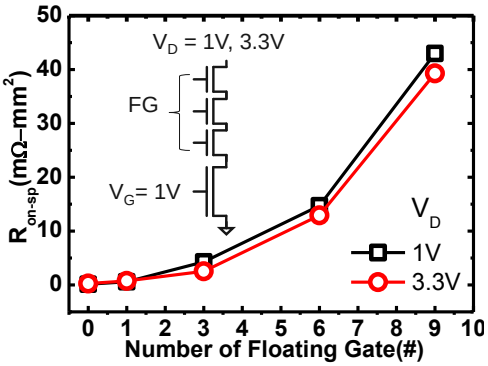

Figure 6 Simulated specific on-resistance degrades greatly as number of FGs exceed 5.

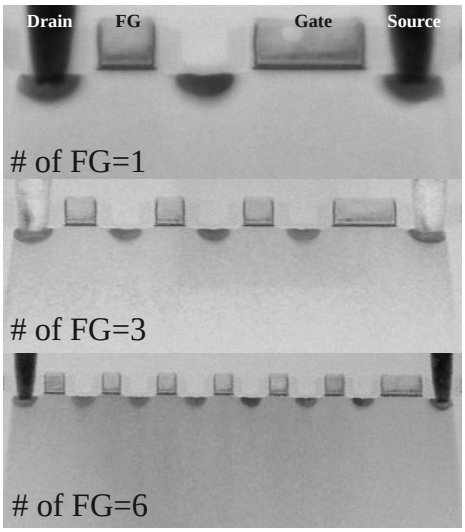

Figure 7 Cross-sectional TEM of the FFP MOSFETs.

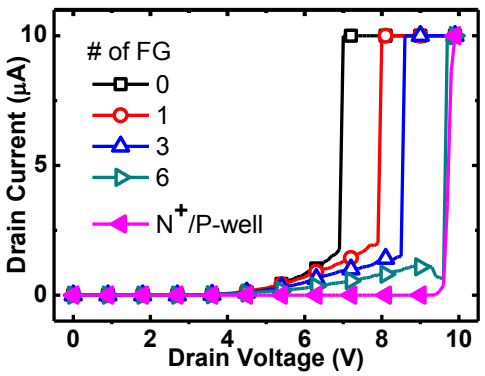

Figure 8 Measured drain breakdown characteristics of different FFP MOSFETs.

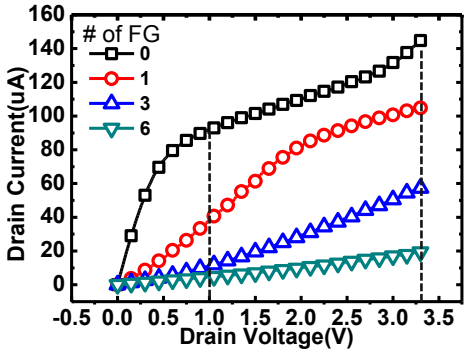

Figure 9 Measured on- characteristics of different FFP MOSFETs

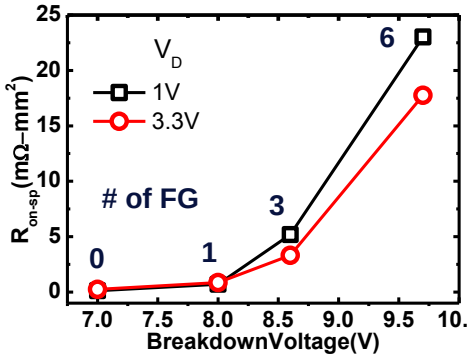

Figure 11 Measured specific on-resistance vs. breakdown voltage for FFP MOSFETs with different number of FG.

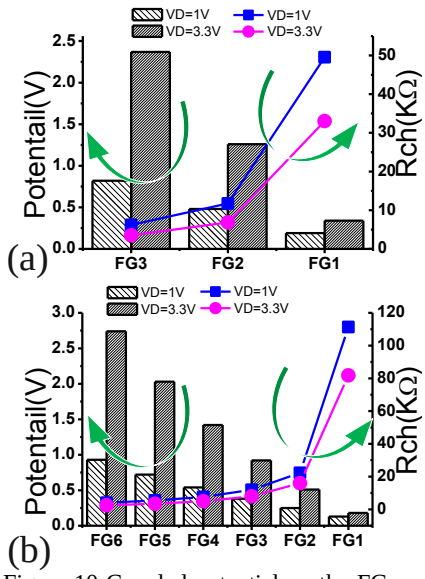

Figure 10 Coupled potential on the FGs and the corresponding channel resistances of (a) number of FG=3, (b)number of FG=6.

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