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An Explicit Compact Model for High-Voltage LDMOS

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Abstract

In this paper, we present an analytical DC model for high-voltage (HV) LDMOS. The proposed model is based on explicit calculations of surface potential, drift resistance and internal drain voltage. LDMOS characteristics such as trans-conductance sharp peak and quasi-saturation are well captured. The model is robust, efficient and showing good agreement with both numerical and measured data.

1. Introduction

Lateral double-diffused MOSFETs (LDMOS) are widely used in applications such as automotive and RF circuits. Numerous compact models have been reported over the past few decades. One approach is to construct a sub-circuit so that its terminal behaviors match the ones of a LDMOS [1]. Another approach is to introduce an internal node between the channel and drift region (K-point) [2-5]. In both cases, iterations are usually required and efforts have to be made to ensure convergence and improve efficiency.

In order to avoid iterations and eliminate any convergence issues, we present a novel analytical approach by introducing a unified regional drift resistance. Separate equations for each operating region can be easily formulated and then unified into a single-piece expression. This enables the explicit calculation of K-point voltage, improves robustness and efficiency of the model.

2. Formulations

The LDMOS device is divided into the channel and drift regions. Applying KCL at the K-point, the following equation can be derived:

$$\mu C_{ox}\frac{W}{L}\left(q_{in,s}-\frac{1}{2}A_{b,s}V_{ks}+V_{th}A_{b,s}\right)\mathrm{V}_{ks}=\frac{V_{ds}-V_{ks}}{R_{drift}} \quad (1)$$

In eq. (1), $q_{in,s}$ is the normalized inversion charge density obtained from the surface potential solution at the source side [6]. R_{drift} is the unified drift resistance calculated by smoothly joining the linear, quasi-saturation and saturation regional resistance, given as

$$R_{drift}=\vartheta_{max}\left(R_{lin},R_{qsat},R_{sat}\right) \quad (2)$$

R_{lin} is the drift region resistance without any lateral field effect. It is modulated by the gate and body bias, and this effect may vary due to the structural differences in LDMOS. R_{qsat} is the high lateral-field drift resistance obtained with the assumption that all the voltage is dropped across the drift region. As reported in [5], the current in drift region may increase beyond saturation. R_{sat} is the resistance beyond linear channel region, and it is proportional to the drain bias with a slope equal to the saturation current. Their expressions are shown below, and they are only valid in their specific regions.

$$R_{lin}=R_{ov}\left(1+V_{gs}\theta_1\right)\left(1+V_{bs}\theta_2\right)+R_{dr}\left(\frac{L_{dr}}{W}\right) \quad (3)$$

$$R_{qsat}=\frac{V_{ds}}{A_f\left(V_{ds}-v_{sat}(L_{ov}+L_{dr})/\mu_{dr}\right)+v_{sat}(L_{ov}+L_{dr})/(R_{lf}\mu_{dr})} \quad (4)$$

$$R_{sat}=\frac{V_{ds}-V_{ds,eff}}{I_{ch}} \quad (5)$$

K-point here is defined at the end of the linear channel instead of the physical point at the body-drift junction, and its voltage can be calculated by solving eq. (1) analytically. Once V_{ks} is obtained, its value can be substituted back into eq. (1) to obtain the drain current.

3. Model Verification

Comparison with TCAD Simulations

In order to verify the compact model, we conducted TCAD simulations to compare IV curves in DC operation. The numerical device has a channel length of 1μm, a gate-overlap length of 1μm and a drift-region length of 2μm. The drift region doping concentration is set to a constant at 1×10^{16} cm^{-3}, and the channel doping peak is set at 1×10^{18} cm^{-3}.

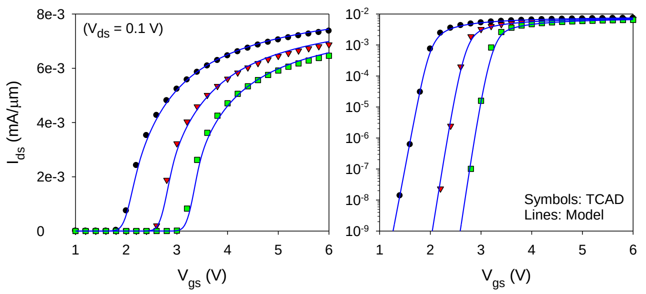

Fig 1. I_{ds}–V_{gs} curves in linear region (V_{ds} = 0.1 V) at V_{bs} = 0, –1, –2 V.

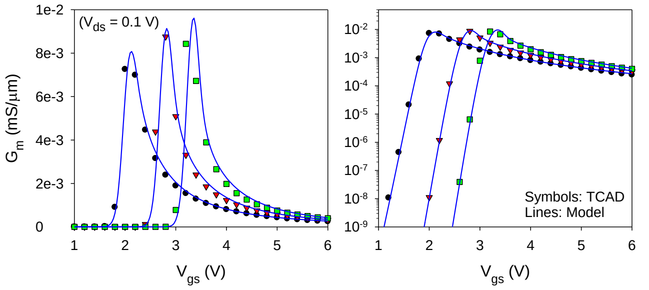

Fig 2. G_m–V_{gs} curves in linear region (V_{ds} = 0.1 V) at V_{bs} = 0, –1, –2 V.

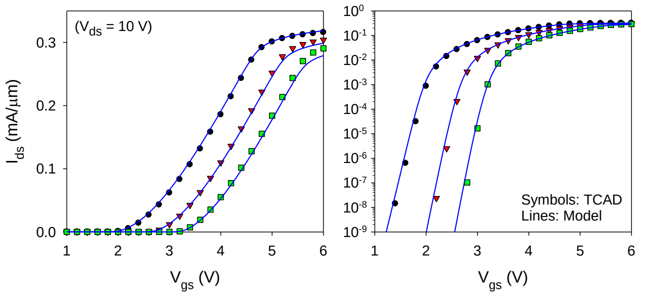

Fig 3. I_{ds}–V_{gs} curves in saturation region (V_{ds} = 10 V) at V_{bs} = 0, –1, –2 V.

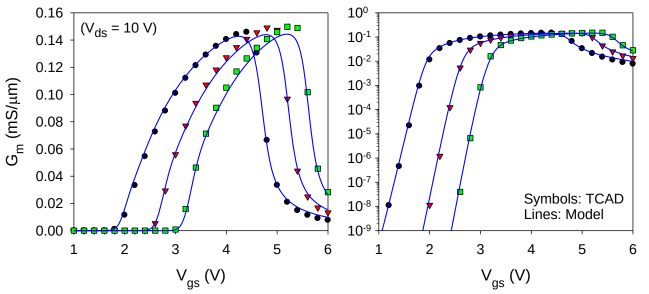

Fig 4. G_m–V_{gs} curves in saturation region (V_{ds} = 10 V) at V_{bs} = 0, –1, –2 V.

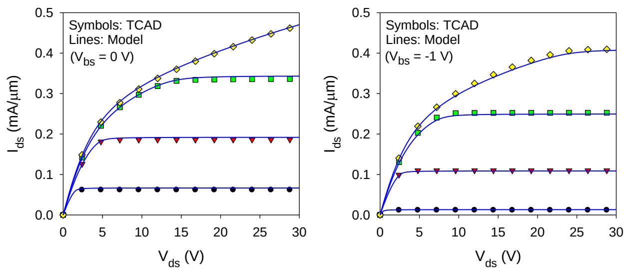

Fig 5. I_{ds}–V_{ds} curves at V_{gs} = 3, 4, 5, 6 V.

Comparison with Measured Data

The model is also calibrated with a 30V-LDMOS device. As shown in the following figures, the calculated current shows excellent consistency with the measured data. In addition, lattice self-heating effect is included through a standard thermal resistor. Substrate current is calculated by considering impact ionization effects in both channel and drift regions.

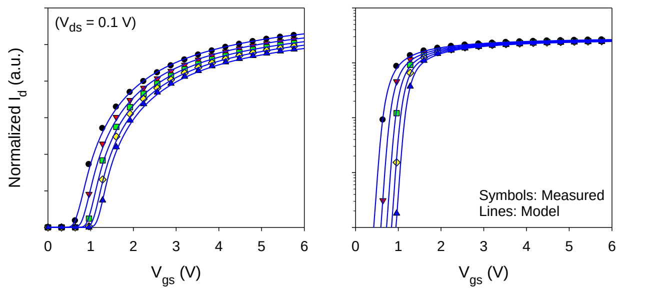

Fig 6. I_d–V_{gs} curves in saturation region (V_{ds} = 0.1 V) at V_{bs} = 0, –0.5, –1, –1.5, –2 V.

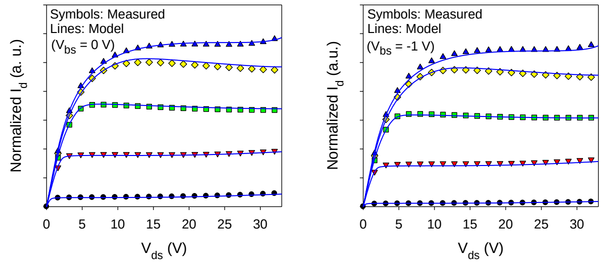

Fig 7. I_d–V_{ds} curves at V_{gs} = 1.2, 2.4, 3.6, 4.8, 6.0 V.

4. Conclusions

In this paper, an explicit compact model for HV-LDMOS is presented. Different from conventional sub-circuit and iterative approaches, expressions for drift resistance are derived for specific regions and later unified. This novel approach enables the explicit calculation of the K-point voltage and terminal current. Without iterations, the model is highly robust and efficient, and its accuracy has been well demonstrated by comparing to both numerical and experimental data.

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