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Role of Carrier Response Delay on Switching Performance of Injection-Enhanced IGBT

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Abstract

The Injection-Enhanced Insulated-Gate-Bipolar Transistor was invented to reduce the on-state voltage. We have successfully developed a compact model describing the hole accumulation in the floating-base region, which causes the negative gate capacitance, the origin of the reduction. This investigation reports that the hole response delay, suppressing the negative capacitance, plays an important role on switching performance for real circuits.

1. Introduction

The Injection-Enhanced Insulated-Gate-Bipolar Transistor (IEGT) structure has been developed in order to reduce the on-state voltage and achieving a smooth switching waveform (soft switching) [1] in comparison to the conventional Insulated-Gate-Bipolar transistor (IGBT). The difference of the two structures is either symmetrical or asymmetrical as depicted in Fig. 1, where one side of the p-base region of IEGT is disconnected and floating.

IEGT has been utilized for applications where reduced voltage overshoot is required. However, the smoothed waveform causes large switching loss. To optimize the trade-off between the low overshoot and the low energy-loss at the same time, accurate circuit simulations valid for investigating the switching performance of IEGT is inevitable.

We have developed the compact model HiSIM-IEGT [2] based on the conventional IGBT model HiSIM-IGBT [3,4]. The main development is modeling the hole accumulation in the floating base. For the purpose we have introduced the potential node V_{fp} (see Fig. 1), which is solved together with other nodes under the Kirchhoff law.

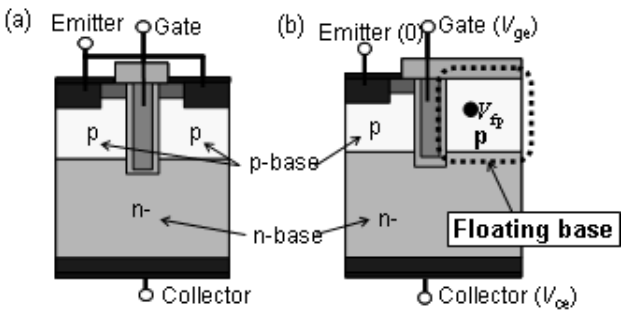

Fig. 1. (a) The symmetrical IGBT structure, and (b) the asymmetrical IEGT structure.

With use of the developed HiSIM-IEGT we investigate here the switching performance of IEGT in comparison to measurements.

2. Measured Switching Response of Floating Base

Fig. 2 (a) shows a switching circuit studied, and Fig. 2 (b) compares measured results to those of simulation with HiSIM-IGBT no inclusion of the hole accumulation effect in the floating base region. It is observed that the measured waveform of the collector current I_c is not as steep as that of IGBT, and thus softer switching behavior is realized.

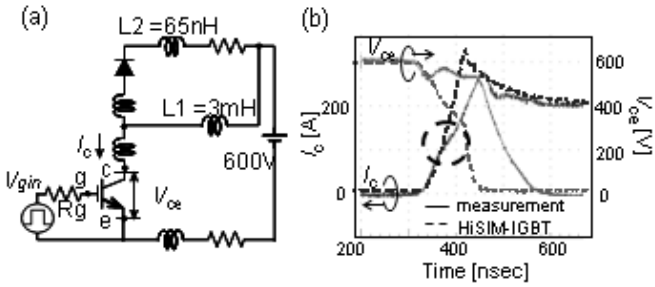

Fig. 2. (a) Studied basic circuit with inductive element values, (b) measured transient characteristics in comparison to simulation results with HiSIM-IGBT without considering the hole accumulation.

Fig. 3 depicts the gate oxide capacitance C_{gg} and the floating-base potential V_{fp} simulated with a 2D device simulator [5]. It can be seen that the large negative C_{gg} of the floating base induced at the floating base contact is the specific feature of IEGT [6, 7], and has been modeled in HiSIM-IEGT successfully [2] (see Fig. 5).

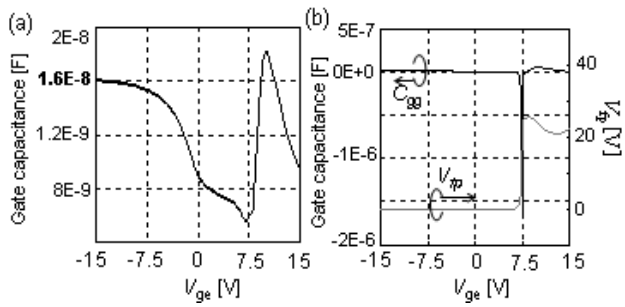

Fig. 3. 2D device simulation results of C_{gg} at V_{ce}=600V, freq=0.001Hz as a function of V_{ge} (a) for IGBT and (b) for IEGT. The floating-base potential V_{fp} is also depicted together.

3. Floating-Base Effect Model and Calculation Result

The floating-base effect is modeled by considering an n-MOS capacitor in addition to HiSIM-IGBT as shown in Fig. 4. The base node V_b as well as V_{fp} are calculated by solving the Kirchhoff law explicitly, namely, $I_c+I_b+I_e=0$ [3,4] The additional equivalent circuit shown in Fig.4 is included in the conventional HiSIM-IGBT and tested with a SPICE simulator. The negative C_{gg} is much larger than the positive C_{gg} as can be seen in Fig.5. The total C_{gg} is dominated by the negative C_{gg} between 7V and 8V, when the hole accumulation occurs. An important task is to calculate the negative C_{gg} accurately.

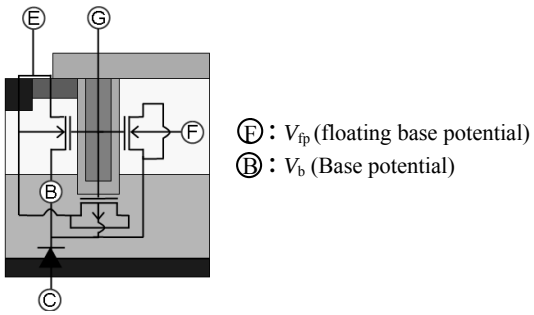

Fig. 4. Equivalent circuit of the developed IEGT model.

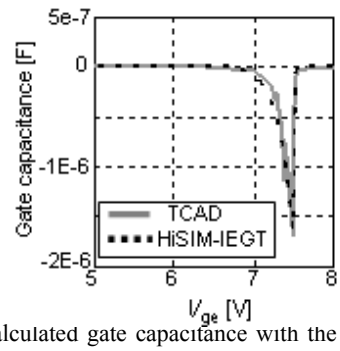

Fig. 5. Calculated gate capacitance with the HiSIM-IEGT model and TCAD simulation result.

Fig. 6 shows the switching waveform simulated with the developed IEGT model including the floating-base effect in comparison to measurement data. The circuit shown in Fig. 2(a) is investigated. It is seen that the measured soft switching behavior observed in the collector current I_c is accurately reproduced. Furthermore, the collector voltage V_{ce} is also well reproduced with change of I_c waveform. However, it has to be noticed that the negative C_{gg} predicted by 2D-device simulations is too large to reproduce the measured wave form (see Fig. 3(b)).

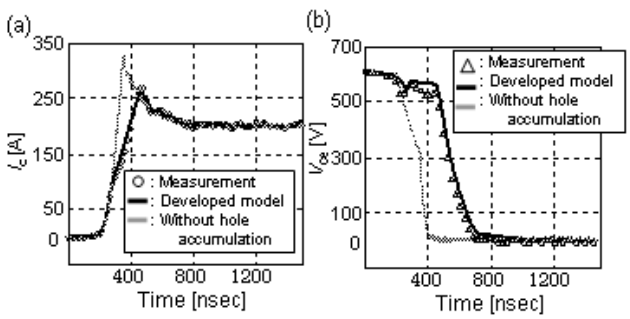

Fig. 6. Comparison of calculated switching turn-on waveform with measured results (a) I_c waveform and (b) V_{ce} waveform.

4. Discussion

Fig. 7 (a) shows frequency dependence of the total C_{gg} as a function of V_{ge}. It is seen that the negative C_{gg} is reduced at high frequency. Fig. 7 (b) shows frequency dependence of the minimum value of the total C_{gg}. The rapid reduction of the negative C_{gg} is observed beyond 1kHz. This frequency dependence of C_{gg} is attributed to the carrier transit delay, causing the device response delay to the switching speed. If the switching is faster than the carrier movement, reduction of C_{gg} is observed due suppressed amount of hole gathered. We have extracted the accumulated hole density of only about a few percents of the total expected hole density. This extracted drastically reduced accumulated hole density is exactly due to the carrier response delay.

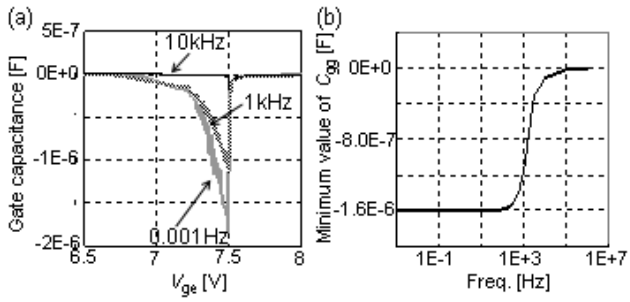

Fig. 7. 2D device simulation result. (a)The V_{ge} voltage dependence of total C_{gg} at V_{ce}=600V. (b) Frequency dependence of the minimum value of total C_{gg} at V_{ce}=600V.

5. Conclusions

A new HiSIM-IEBT model has been developed, which consider the floating-base effect. This model has been implemented in a circuit simulator and verified to be accurate. The characteristics switching waveform seen for the IEGT structure has also been accurately reproduced in the circuit simulation. It becomes clear that the negative capacitance has frequency dependent.

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References

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