Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp38-39

Young Modulus of Si in 3D-LSIs and Reliability

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1. Introduction and Experiment

The global mobile data traffic trend reveals that the total amount of data exchanged via internet might exceed the 10 exabytes (EB, 1EB = 1000 petabytes) level per month in the near future, by 2016. At the same time the number of overall hand-held electronic gadgets touched the 10 billion units in 2010, revealing that a considerable portion of the data-transfer is taking place via the mobile units. The video/web data is the mostly exchanged data type using the mobile electronic gadgets. So the integrated circuit system will consist nearly ten times more devices in the future mobile units to minimize the usage friction along with improved user interface, but this has to be achieved in a smaller form factor and at lower cost. The one and only way to achieve it in a smaller from factor is the three dimensional (3D) – integration of various LSIs (large scale integrated chip) [1]. This method (fig. 1) consists of the following three key processes such as (i) die/wafer thinning (ii) formation of metal-interconnects (though-silicon-via, TSV and μ-bump), and (iii) injection of an organic underfill into the interlayer gap. Both TSVs and μ-bumps are used for electrical interconnections, whereas the organic underfill is injected between the stacked LSI dies for mechanical rigidity.

The main advantage of 3D-Integration is the minimum interconnect length which is not possible either in 2D or 2.5D. The parasitic capacitance in 3D is about 0.7 pF, where is it is 6 and 20 pF for 2.5D and 2D [2]. Almost the thickness of the LSI die forms the interconnect length in 3D. Therefore to reduce the parasitic capacitance and to obtain reliable interconnects, it is wise to keep the die/wafer as minimum as possible. On the contrary, the die/wafer thinning process either makes the ultra-thin die/wafer to suffer from the residual stress or eliminates the gettering layer for heavy metal atoms coming from BEOL process. We have already demonstrated several reliability issues associated with the 3D-LSI process such as the stress-relief method dependent residual stress in 3D-LSIs [3], diffusion of Cu atom (from back metal contamination) into the active Si [3], the large CTE (co-efficient of thermal expansion) difference (between the metal (the CTE of Cu is ~$17x10^{-6}$/K of the metal-filled TSVs and μ-bumps is much greater than the CTE of Si ~$2.6x10^{-6}$/K) induces severe themo-mechanical stress in the active Si[4] and the CTE difference between Si and the organic under-fill renders the 3D-LSIs to deform and thus causing the local mechanical stress around the microbump region [5,6].Apart from the above mentioned reliability concerns, one may expect a reliability problem associated with the lattice mis-orientation caused by local deformation of the LSI die in 3D-LSIs. It was shown by us that as high as around one degree of lattice orientation in the stacked LSI dies using an array of microbumps [7].

In this paper, we focus our attention to the mechanical properties of the stacked die/wafer in 3D-LSIs. It is worth to mention that in all finite element model (FEM) analysis of themo-mechanical stress induced by Cu-TSVs in the adjacent Si is carried out using the Young modulus (E) value of 165 – 180 GPa, depending upon the Si orientation. If one consider the surface plane of Si wafer as (100) direction, then for the "*X*- or *Y* -axis" direction (parallel/perpendicular to flat surface), the E_{110} value of 169 GPa is normally used. The maximum *E* value in silicon is 190 GPa, which occurs in the <111> direction, and the minimum value is 130 GPa, in the <100> direction [8]. However, it is not the case with the ultra-thin Si with thicknesses in order of few tens of micrometer. It is has been shown by that the E value of 5 um-thick implantable Si is around 5 GPa [9]. Further, the choice of *E* value can have a significant influence on the result of FEM analysis as proven by Hopcroft *et al* in [10]. It was shown by them that the discrepancy may be as little as 5% (by using E value as 160 GPa instead of 169 GPa) or as much as 46% (by using E value as 190 GPa instead of 130 GPa) in the FEM results.

In high-density 3D-LSIs since it is a prerequisite to have a thinned Si, it is important to study their mechanical properties. The mechanical properties such as E and the hardness, H, of ultrathin die/wafer stress relieved by various methods (chemical mechanical polishing CMP, plasma etching PE, ultra-poly grinding UPG, poly grinding PG, dry polishing DP, and #2000) were studied by nano-indentation method.

2. Experiment and Results

Shown in Fig. 1 is the schematic view of cross-section for the high-density 3D-LSIs. The nano-indenter tip of pyramid geometry is projected into the selected location on 3D-LSI wafer surface. The load is continuously increased to a designated maximum value. Next holding segment is introduced to allow the material to relax before unloading. The process is repeated four times for four different applied load, and the position of the indenter tip on the surface is monitored with a capacitance meter.

Shown fig. 2, 3 and4 are respectively the 2D-IPF mapping obtained by EBSD, the high resolution TEM images, and AFM images obtained for 50 μm-thick LSI wafer stress relieved by CMP and DP. In the case of DP, the presence of damaged Si layer was confirmed by all the three (EBSD, TEM and AFM) analysis. In our previous studies we had shown the existence of correlation between the residual stress and the residual stress or otherwise the damaged Si.

Fig. 5 and fig. 6 show respectively the variation of Young modulus with type of stress-relief method and the wafer thickness. From fig. 5 it is clear that the CMP processed wafer with 30 micrometer thickness retains the higher Young modulus and hardness values as compared to the 30 micrometer-thick wafer stress relieved by dry-polishing. Even for the 100 μm-thick 3D-LSI die both E and H decreased with an increase in the applied load (from 24 mN to 196 mN). Among IG, P/P+, P/P- wafers, IG wafer had very low E (142 GPa) and H (10 GPa), whereas P/P- possessed the relatively large E (172 GPa) and H (11.5 GPa) values. Therefore care must be taken while introducing the IG layer either via implantation or by differential thermal treatment method. For wafer/die thickness of anything less than 50 μm leads to a many fold decrease in E and H values. For example, for the die thickness of 100/50 μm the DP wafer showed the E value of 172 GPa, where as it was suppressed to < 30 GPa for the thickness of 30 μm. It is worth to notice that regardless of the thickness of the LSI dies, the CMP processed LSI die maintains higher E and H values among several types of stress-relieved wafers. On contrary, the mechanical properties were found to be very poor for the DP and PE dies.

3. Summary

E and H of thin-LSI dies (10 mm x 10 mm) carved-out from 300 mm LSI wafer were examined for their mechanical properties with respect to different stress-relief processes via nano-indentation method. We found that there exists a good correlation between the residual stress present in the die/wafer and the Young modulus of the respective die/wafer. Among the variously stress-relieved wafers, the chemically-mechanically polished die/wafer possessed the minimum residual stress and large E and H values. While the die/wafer stress relieved by dry polishing method possessed larger residual stress-values, and small E and H values. Upon comparing the E values obtained for variously stress relieved LSI die/wafer for different die/wafer thicknesses to the E values of bulk Si (*E*111 = 188 GPa *; E*110 = 169 GPa*; E*100 = 130 GPa) [5], it is clear that the CMP processed thin-LSI die/wafer had better mechanical properties, which is highly important to achieve the high-performance 3D_LSI with enhanced reliability. It is inferred from various data that one can improve the mechanical strength and minimize the reliability risks involved in the 3D-LSIs by appropriately stress-relieved die/wafer for integration.

References

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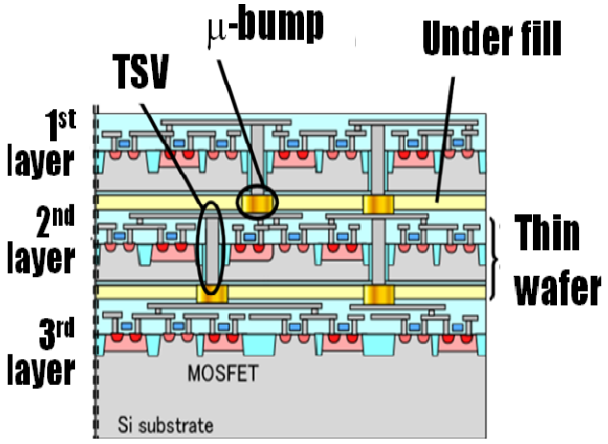

Fig. 1: Schematic cross-sectional view of vertically stacked 3D-LSI using metal μ-bumps and TSVs

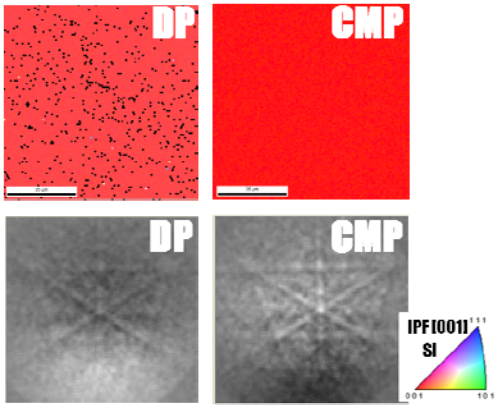

Fig. 2: 2D-IPF image (top) and Kikuchi lines (bottom) obtained for dry polished (left) and chemical-mechanical polished (right) Si chips.

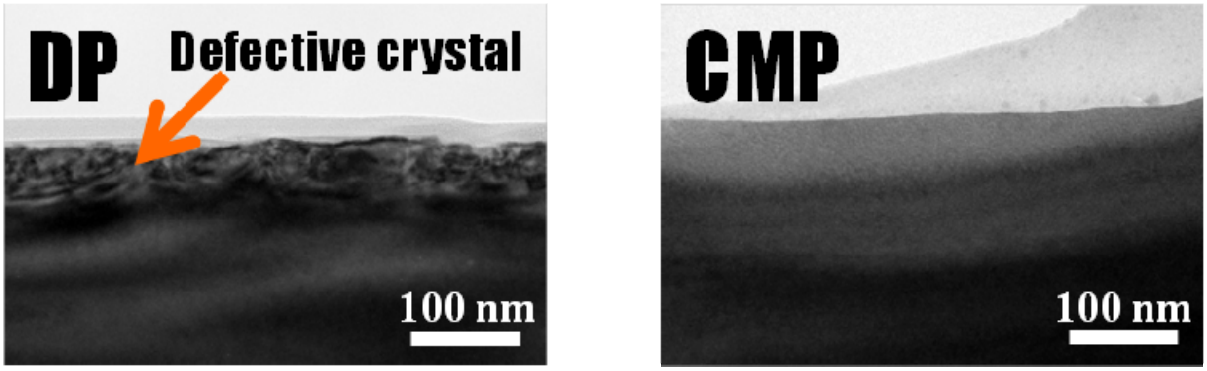

Fig. 3: HRTEM image obtained over 50 μm-thick Si wafer stress relieved by dry polishing (left) and chemical-mechanical polishing (right) after back grinding

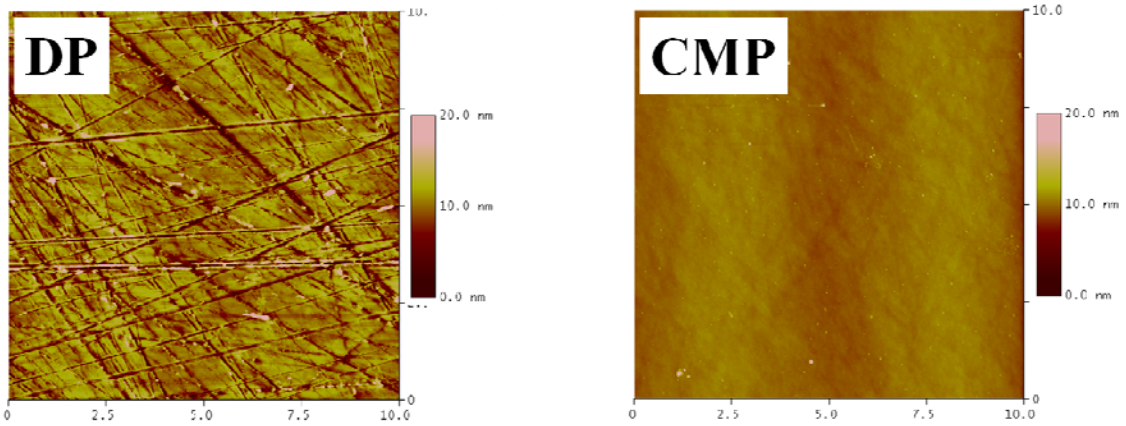

Fig. 4: AFM images obtained over 50 μm-thick Si wafer stress relieved by dry polishing (left) and chemical-mechanical polishing (right) after back grinding

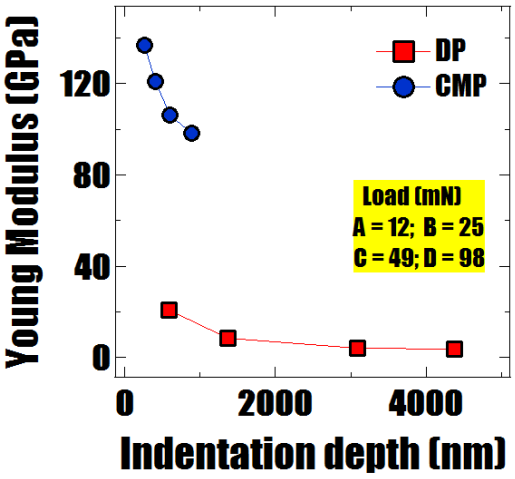

Fig. 5: Stress-relief dependent Young modulus for 30 μm-thick LSI wafer.

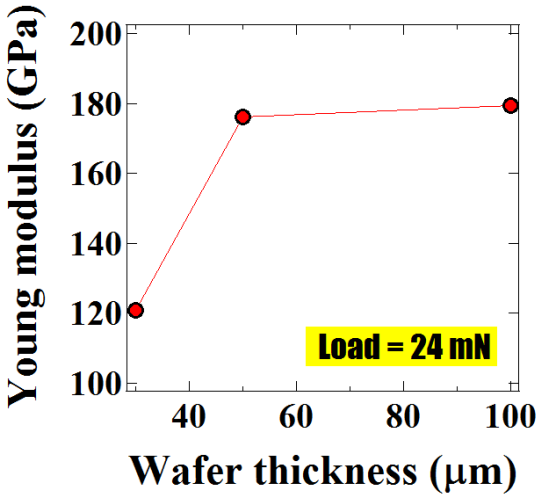

Fig. 6: Thickness dependent Young modulus of LSI wafer stress relieved by chemical-mechanical polishing.