Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp76-77

Understanding HCI Variability in Deeply Scaled nMOSFETs

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1. Introduction

Hot carriers injection (HCI) degradation has been recognized as the one of the most important reliability issues for nMOSFETs. With scaling down, HCI degradation becomes worse, on the other hand, hot carrier (HC) induced device parameter variability is getting serious [1-3]. Understanding the variability will be crucial for correctly predicting the degradation behavior and lifetime in deeply scaled technology [4]. In this work, we investigate HC induced device parameter variability with scaling down. The purpose of this paper is to understand the physical origin of large HCI variability in deeply scaled devices.

2. HCI variability with scaling down

The experimental analysis was carried out on nMOSFETs with the technology nodes from 0.35μm to 45nm. To gather the process variation, five lots with about 90 cells in each node were selected. Before investigating HCI lifetime, we first studied the worse case condition after HCI stress of these devices. As seen in Fig.1, devices scaling changes the worse stress condition from I_{bmax} to $V_g = V_d$. Fig.2 shows the time behaviors of I_{dsat} shifts (δI_{dsat}) under the worse case condition for seven 45nm devices. Even though all δI_{dsat} exhibit power law time exponent (t^n) with n about 0.4-0.5, δI_{dsat} variability is large when t is below 200s. Furthermore, the stress is smaller, δI_{dsat} variability is larger.

Based on the estimated δI_{dsat} values at 10% of I_{dsat0}, HCI lifetime is evaluated with a multi-parameters (size, voltage, temperature) model for each technology node [5]. Fig.3 and Fig.4 shows the obtained cumulative probability for HCI lifetime in the 65nm and 45nm devices, respectively. All HCI lifetimes follow the Log-normal distribution. It is clearly seen that 45nm devices have larger log-normal standard deviation ($\sigma(T_{50})$) than 65nm devices. Fig.5 and Fig.6 show the correlation between the median (T_{50}) and $\sigma(T_{50})$ with the channel length in the range of 0.35 μm to 45nm. It is seen that T_{50} continuously decreases with reducing the channel length, on the other hand, the larger lifetime deviation $\sigma(T_{50})$ is observed in the smaller device.

3. Origin of large HCI variability in scaled devices

Comparing the results of Fig. 2 with Fig. 4, it is considered that the large HCI lifetime deviation in 45nm device is due to the large δI_{dsat} variability. To understand δI_{dsat} variability, the statistical analyses for the saturation current degradation were carried out. Fig. 7 shows the correlation between the initial I_{dsat0} and δI_{dsat} after 10s HC stress. The lack of the correlation of I_{dsat0} and δI_{dsat} allow us to study HCI generated trap fluctuation independently with the process fluctuation due to the effects such as random doping fluctuation, line edge roughness. Fig.8 shows the cumulative probability of δI_{dsat} verse the stress time for 45nm devices. We note that $\sigma(\delta I_{dsat})$ decreases with the stress time. Fig. 9 shows the relationship of $\sigma(\delta I_{dsat})$ and $\mu(\delta I_{dsat})$ at various HCI stress. All the experimental data fall on one curve, $\sigma(\delta I_{dsat})$ described by:

$$\sigma(\delta I_{dsat}) = \frac{A}{(\mu(\delta I_{dsat}))^n} \qquad (1)$$

here n is about 0.4 for 45 nm device. As $\mu(\delta I_{dsat})$ directly corresponds to the amount of the traps number generated by HC stress, Euq.1 illustrates that the smaller amount of the trap number, the larger δI_{dsat} variability. As the standard deviation of the HC-induced δI_{dsat} is proportional to $\mu(\delta I_{dsat})$, it is considered that $\sigma(\delta I_{dsat})$ is mainly dominated by the Poisson-distribution in number. Recently, NBTI stress-induced parameter variability is argued to be a convolution of exponential distributions of uncorrelated individual charged defects Poisson-distributed in number. Combined with both distributions, the variability of stress-induced parameter shift should increase with decreasing the mean number of defects. The same model proposed for the case of NBTI stress could be valid for HC induced parameter mismatch. The only difference is that the NBTI stress effects are assumed uniform along the channel whereas HC stress effects are characterized by a strong non-uniformity. Here, we could assume that interface and oxide traps are generated in a region (W X L_{HC}) with L_{HC} =L/K; Fig.10 shows the measured trap distributions along the channel after HCI stress for deeply scaled nMOSFETs by threshold voltage fluctuation method[6]. It is seen that the charged region in HCI degradation is about half of the channel length, informing that the value of K is about 2 in deeply scaled devices. Fig. 11 shows the relationship of $\sigma(\delta I_{dsat})$ and $\mu(\delta I_{dsat,})$ at various HCI stress for various technology nodes. The results show that the parameter A in Equ.1 is dependent with the process but n is almost same for all technology nodes. We can use Equ.1 to predict the HC-induced variability for different technology nodes.

4. Conclusion

The HCI induced $\sigma(\delta I_{dsat})$ and $\sigma(T_{50})$ has been investigated for nMOSFETs. It is found that the HCI variability is getting worse with scaling down. The statistical analyses are applied and the physical models are proposed to explain the scaling properties of observed HCI parameter variability.

Acknowledgements

This work was supported by 973 Program of China (No. 2010CB934200, 2012CB619200).

References

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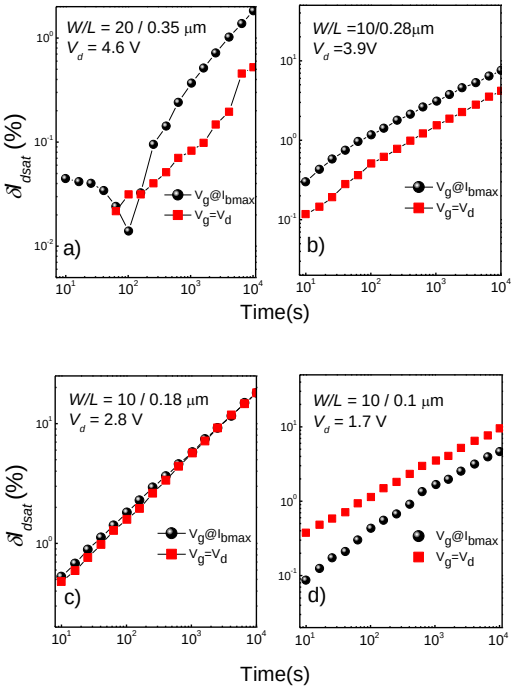

Fig.1 δI_{dsat} degradation at condition of $V_g@I_{bmax}$ and $V_g=V_d$ for a)0.35μ m, b)0.28μ m, c)0.18μ m, d)0.1μ m. $V_g@I_{bmax}$ is the worst case condition for devices with L>0.18μm, and $V_g=V_d$ is the worst case condition for devices with L≤ 0.1μm.

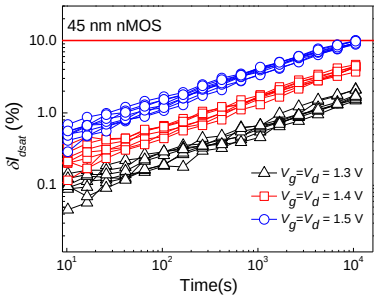

Fig.2 Power law time exponent dependence of δI_{dsat} degradation in 45nm devices. The δI_{dsat} variation is large at the first 200s.

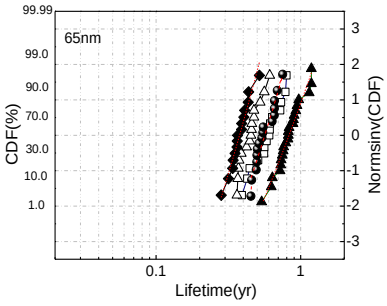

Fig.3 Cumulative probability of HCI lifetime for 65 nm devices. HCI lifetime follows the Log-normal distribution.

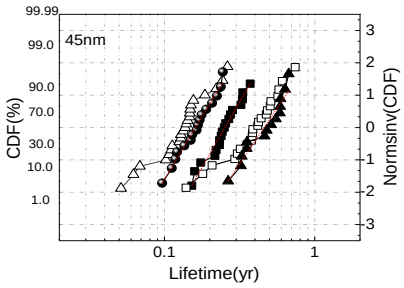

Fig.4 Cumulative probability of HCI lifetime for 45 nm devices. There is a larger log-normal standard deviation comparing to 65nm device

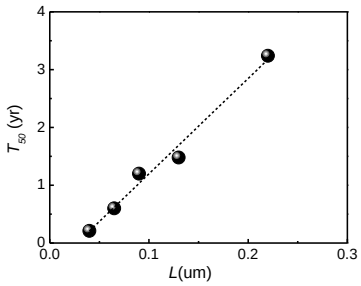

Fig.5 The median of HCI lifetimes (T_{50}) versus channel length. There is a lower lifetime (T_{50}) for shorter devices. The lifetime exhibits a linear dependence with channel length.

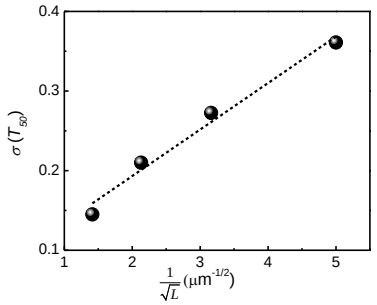

Fig.6 The variability of HCI lifetimes (T_{50}) versus channel length, the deviation $\delta(T_{50})$ is lager for shorter devices.

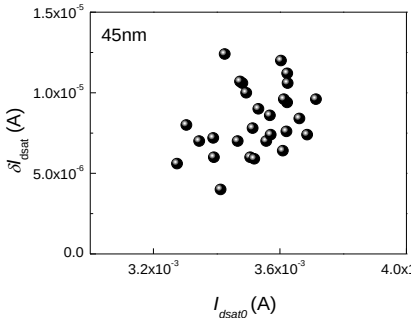

Fig.7 The correlation between I_{dsat0} and induced δI_{dsat} after 10s HCI stress. No strong correlation between δI_{dsat} and I_{dsat0} is found.

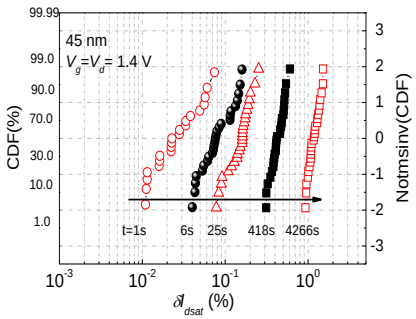

Fig. 8 Log-normal distribution for δI_{dsat} at various stress time. It is seen that the small amount of the trap number results in the large δI_{dsat} variability.

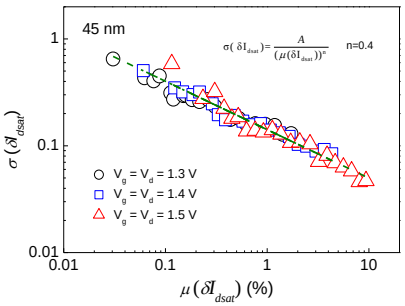

Fig. 9 The variability versus median of δI_{dsat} under various HCI stress. The dashed line is the prediction from the equation $\sigma(\delta I_{dsat})=\frac{A}{\mu(\delta I_{dsat})^n}$, here n=0.4.

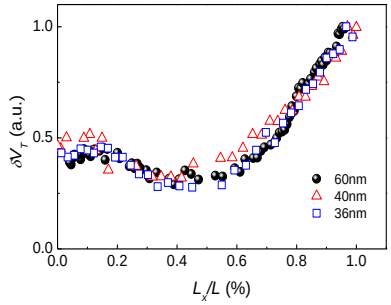

Fig. 10 The traps distribution along the channel after HCI stress in 60nm, 40nm and 36nm devices by threshold voltage fluctuation technology. The changed region in HCI degradation is about half of the channel length

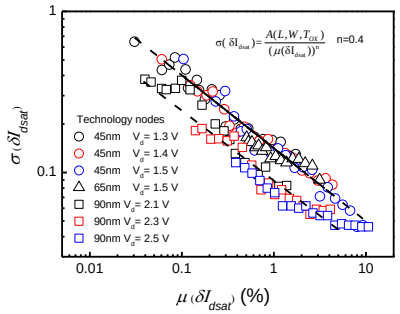

Fig. 11 The variability versus median of δI_{dsat} for different channel length devices. The dashed line is the prediction from the equation. For different technology nodes, n is the same while A is related to the process parameter.