Understanding HCI Variability in Deeply Scaled nMOSFETs

Lijuan Ma¹, Xiaoli Ji¹, Zhaoxing Chen², Yiming Liao², Feng Yan¹, Yongliang Song³, Qiang Guo⁴
¹Nanjing University, China ²SanDisk Information Technology Co. Ltd. ³SMIC, China ⁴WXSMC, China.

Email: xji@nju.edu.cn; fyan@nju.edu.cn

1. Introduction
Hot carriers injection (HCI) degradation has been recognized as the one of the most important reliability issues for nMOSFETs. With scaling down, HCI degradation becomes worse, on the other hand, hot carrier (HC) induced device parameter variability is getting serious [1-3]. Understanding the variability will be crucial for correctly predicting the degradation behavior and lifetime in deeply scaled technology [4]. In this work, we investigate HC induced device parameter variability with scaling down. The purpose of this paper is to understand the physical origin of large HCI variability in deeply scaled devices.

2. HCI variability with scaling down
The experimental analysis was carried out on nMOSFETs with the technology nodes from 0.35µm to 45nm. To gather the process variation, five lots with about 90 cells in each node were selected. Before investigating HCI lifetime, we first studied the worse case condition after HCI stress of these devices. As seen in Fig.1, devices scaling changes the worse stress condition from \( I_{\text{max}} \) to \( V_g = V_{d} \). Fig.2 shows the time behaviors of \( I_{\text{dsat}} \) shifts (\( \delta I_{\text{dsat}} \)) under the worse case condition for seven 45nm devices. Even though all \( \delta I_{\text{dsat}} \) exhibit power law time exponent (t\(^n\)) with n about 0.4-0.5, \( \delta I_{\text{dsat}} \) variability is large when t is below 200s. Furthermore, the stress is smaller, \( \delta I_{\text{dsat}} \) variability is larger.

Based on the estimated \( \delta I_{\text{dsat}} \) values at 10% of \( I_{\text{dsat0}} \), HCI lifetime is evaluated with a multi-parameters (size, voltage, temperature) model for each technology node [5]. Fig.3 and Fig.4 shows the obtained cumulative probability for HCI lifetime in the 65nm and 45nm devices, respectively. All HCI lifetimes follow the Log-normal distribution. It is clearly seen that 45nm devices have larger log-normal standard deviation (\( \sigma(T_{\text{sh}}) \)) than 65nm devices. Fig.5 and Fig.6 show the correlation between the median (\( T_{\text{sh}} \)) and \( \sigma(T_{\text{sh}}) \) with the channel length in the range of 0.35 µm to 45nm. It is seen that \( T_{\text{sh}} \) continuously decreases with reducing the channel length, on the other hand, the larger lifetime deviation \( \sigma(T_{\text{sh}}) \) is observed in the smaller device.

3. Origin of large HCI variability in scaled devices
Comparing the results of Fig. 2 with Fig. 4, it is considered that the large HCI lifetime deviation in 45nm device is due to the large \( \delta I_{\text{dsat}} \) variability. To understand \( \delta I_{\text{dsat}} \) variability, the statistical analyses for the saturation current degradation were carried out. Fig. 7 shows the correlation between the initial \( I_{\text{dsat0}} \) and \( \delta I_{\text{dsat}} \) after 10s HCI stress. The lack of the correlation of \( I_{\text{dsat0}} \) and \( \delta I_{\text{dsat}} \) allow us to study HCI generated trap fluctuation independently with the process fluctuation due to the effects such as random doping fluctuation, line edge roughness. Fig.8 shows the cumulative probability of \( \delta I_{\text{dsat}} \) verse the stress time for 45nm devices. We note that \( \sigma(\delta I_{\text{dsat}}) \) decreases with the stress time. Fig. 9 shows the relationship of \( \sigma(\delta I_{\text{dsat}}) \) and \( \mu(\delta I_{\text{dsat}}) \) at various HCI stress. All the experimental data fall on one curve, \( \sigma(\delta I_{\text{dsat}}) \) described by:

\[
\sigma(\delta I_{\text{dsat}}) = \frac{A}{\mu(\delta I_{\text{dsat}})}
\]

here n is about 0.4 for 45 nm device. As \( \mu(\delta I_{\text{dsat}}) \) directly corresponds to the amount of the traps number generated by HC stress, Eq.1 illustrates that the smaller amount of the trap number, the larger \( \delta I_{\text{dsat}} \) variability. As the standard deviation of the HC-induced \( \delta I_{\text{dsat}} \) is proportional to \( \mu(\delta I_{\text{dsat}}) \), it is considered that \( \sigma(\delta I_{\text{dsat}}) \) is mainly dominated by the Poisson-distribution in number. Recently, NBTI stress-induced parameter variability is argued to be a convolution of exponential distributions of uncorrelated individual charged defects Poisson-distributed in number. Combined with both distributions, the variability of stress-induced parameter shift should increase with decreasing the mean number of defects. The same model proposed for the case of NBTI stress could be valid for HCI induced parameter mismatch. The only difference is that the NBTI stress effects are assumed uniform along the channel whereas HCI stress effects are characterized by a strong non-uniformity. Here, we could assume that interface and oxide traps are generated in a region (W X L\(_{\text{HC}}\)) with L\(_{\text{HC}}\) =L/K; Fig.10 shows the measured trap distributions along the channel after HCI stress for deeply scaled nMOSFETs by threshold voltage fluctuation method[6]. It is seen that the charged region in HCI degradation is about half of the channel length, informing that the value of K is about 2 in deeply scaled devices. Fig. 11 shows the relationship of \( \sigma(\delta I_{\text{dsat}}) \) and \( \mu(\delta I_{\text{dsat}}) \) at various HCI stress for various technology nodes. The results show that the parameter A in Equ.1 is dependent with the process but n is almost same for all technology nodes. We can use Eq.1 to predict the HC-induced variability for different technology nodes.

4. Conclusion
The HCI induced \( \sigma(\delta I_{\text{dsat}}) \) and \( \sigma(T_{\text{sh}}) \) has been investigated for nMOSFETs. It is found that the HCI variability is getting worse with scaling down. The statistical analyses are applied and the physical models are proposed to explain the scaling properties of observed HCI parameter variability.

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References
The variability of HCI lifetimes ($T_{50}$) versus channel length, the deviation $\delta(T_{50})$ is larger for shorter devices.

The correlation between $I_{dsat}$ and induced $\delta I_{dsat}$ after 10s HCI stress. No strong correlation between $\delta I_{dsat}$ and $I_{dsat}$ is found.

The traps distribution along the channel after HCI stress in 60nm, 40nm and 36nm devices by threshold voltage fluctuation technology. The changed region in HCI degradation is about half of the channel length.