Effect of dynamic stress on OFF leakage of nanoscale pMOSFETs at high temperature

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Abstract

This paper investigates the degradation of the off leakage current $I_{off}$ under a dynamic stress which appears in nanoscale pMOSFETs. Experimental results showed that OFF-state stress in the dynamic stress generated negative oxide charges $N_{ox}$ in a drain edge and a shallow trench isolation(STI). $N_{ox}$ was the dominant cause of the shift of $I_{off}$, $\Delta I_{off}$, and $\Delta I_{off}$ increased when channel length $L$ was short. Moreover $N_{ox}$ in the STI was hard to recover. As a result, $I_{off}$ under the dynamic stress increases significantly at the short channel pMOSFETs. These observations indicate that the effect of the dynamic stress in pMOSFETs on $I_{off}$ increases with scaling down of $L$. Thus, the dynamic stress in pMOSFETs should be seriously considered when evaluating the short channel pMOSFETs.

1. Introduction

CMOS inverters are widely used owing to a low cost, a high power efficiency, and a high density. CMOS inverters operate with alternating a gate voltage $V_g$ and a drain voltage $V_d$ and a high temperatures atmosphere. Due to the operating condition, negative bias temperature instability (NBTI) is considered as the most serious reliability problem of pMOSFET. NBTI occurs during the ON-state period ($V_g = V_{str}$, $V_d = 0$), and generates interface traps $N_i$ and positive oxide traps [1-3].

Several researchers reported that the defects induced by NBTI are partially recovered during the OFF-state period ($V_g = 0$ V, $V_d = V_{sub}$) [4-5]. However, when the channel length is scaled down, defects are generated during the OFF-state stress. Lee et al. reported that the OFF-state stress induces negative electron charges $N_{ox}$ and interface traps $N_i$ at the drain edge. These traps lead to the shift of the threshold voltage $V_{th}$ and $I_{off}$ within the temporary time [6].

Recently, some of researchers reported that electron traps are generated in the shallow trench isolation (STI) of the near drain [7-8]. This is caused by hot electron induced punch through (HEIP) which is similar with the OFF-state stress condition. Electron traps in the STI causes the hump in the drain current $I_d$ vs $V_g$ curve and reduce the effective channel length. Especially, this effect is more serious in the short width pMOSFETs [8]. In the sub-micron pMOSFET device, $I_{off}$ increases substantially when the electrons are trapped in the STI.

This paper investigates that reliability of the sub-micron channel pMOSFET under dynamic stress which alternates ON-, OFF-state. Moreover, the effect of electron traps in STI generated by OFF-state stress is considered.

2. Experimental Result

The pMOSFET for the experiment were fabricated by using sub-28nm CMOS technology. The devices were p+ poly-Si gate pMOSFETs with gate lengths of 0.054-0.065 $\mu$m and gate widths of 0.25-10 $\mu$m. The equivalent oxide thickness of the SiON gate dielectric is 2.2 nm. The ON-state stress condition is $V_g = -2.8$ V, $V_d = V_{sub} = 0$ V (source voltage $V_s$, substrate bias $V_{sub}$), at a temperature $T = 125$ °C. And OFF-state stress condition is $V_g = -2.8$ V, $V_d = V_{sub} = 0$ V at $T = 125$ °C. The stress voltage periodically is interrupted to measure $V_{th}$, $I_{off}$ using a B1500a semiconductor device analyzer. $V_{th}$ was defined as the $V_g$ at the $I_d = 2$ $\mu$A/mm. $I_{off}$ is defined as drain current at $V_g = 0$ V, $V_d = -2$ V.

The ON-state stress and the OFF state stress were subjected to pMOSFET with $L = 54$ nm. During the ON-state stress, $|\Delta V_{th}|$, shifts of the subthreshold slope $\Delta SS = \frac{\partial V_{th}}{\partial \log I_{d}}$ and positive $N_{ox}$, extracted using the mid-gap voltage method [9] were increased (Fig. 1, and inset). These changes coincide with the typical NBTI degradation which creates donor-like $N_i$ and positive $N_{ox}$. While OFF-state stress was applied, $|\Delta V_{th}|$ which was increased during the ON-state stress was decreased, whereas $\Delta SS$ was increased continuously. Negative $N_{ox}$ were also increased significantly. Although, $N_i$ is monitored by the variation of $\Delta SS$, $\Delta SS$ doesn’t reflect the effects of $N_i$ completely in this case of OFF-state stress due to the negative $N_{ox}$ in the STI. Negative $N_{ox}$ can be generated in the drain edge and the STI which is close to the channel region during the OFF-state stress. Negative $N_{ox}$ in the STI induce the hump in the subthreshold drain current region [8] and are hard to be detrapped by any bias conditions. To investigate the effect of $N_{ox}$ in the STI, $I_d$ of devices with different $W$s was measured. $I_d$ of $W = 0.25$ $\mu$m had the bigger hump than that of $W = 2$ $\mu$m, 10 $\mu$m after OFF-state stress (Fig. 2). Negative $N_{ox}$ in the STI, which are near the channel edge, cause the parasitic channel [7]. As the $W$ of the pMOSFET was decreased, the channel region was more affected by the parasitic
channel. Consequently, the effect of negative $N_{ox}$ in the STI becomes a serious problem in small width devices. When OFF-, ON-states stresses were applied to the pMOSFET, $\Delta V_{th}$ was degraded during the stress, however gate-drain overlap current $\Delta I_{gd}$ was rarely degraded by the OFF-state stress (Fig. 3 and inset). This experimental observation indicates that defects are more generated in the STI than in the drain edge of channel region.

The shifts of $I_{off}$ caused by the dynamic stress were observed for the pMOSFET with $L = 54$, $65$ nm and $W = 2$, $10$ $\mu$m (Fig. 5). $I_{off}$ of the $L = 54$ nm device was increased more than that of $L = 65$ nm device. This observation is similar with currently reported result [6]. $I_{off}$ of $W = 2$ $\mu$m device was also increased greatly compared to that of $W = 10$ $\mu$m device. The cause of the phenomenon was negative $N_{ox}$ in STI.

The degradation of $\Delta I_{off}$ and $|\Delta V_{th}|$ by the dynamic stress with AC condition were observed for the pMOSFET with $W/L = 2$ $\mu$m/54 nm (Fig. 5). The shift of $I_{off}$ is faster than $|\Delta V_{th}|$. This result indicates that $I_{off}$ under dynamic stress in small dimension pMOSFETs should be considered.

3. Conclusions

The effects of the dynamic stress on the small dimension of pMOSFETs are investigated. Negative $N_{ox}$, which are generated during the OFF-state, trapped in the STI augmented $I_{off}$ significantly in condition of the dynamic stress. This effect of negative $N_{ox}$ increased in small dimension pMOSFETs. Especially, as the width of pMOSFET was decreased, negative $N_{ox}$ had more influence on the device. The degradation of $I_{off}$ was more serious than that of $|\Delta V_{th}|$ under dynamic stress with the AC condition. These experimental observations suggest that as pMOSFETs scaled down continuously, $\Delta I_{off}$ should be considered for predicting the lifetime of small width pMOSFETs.

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References