Trap-Assisted Tunneling on Extended Defects in Tunnel Field-Effect Transistors

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Abstract
The effect of defined numbers and types of dislocations in the near intrinsic region of TFETs is analyzed for the first time. Different trap-assisted tunneling mechanisms are identified. Their dependence on \( V_{DS} \) and \( V_{GS} \) is demonstrated.

1. Introduction
Tunnel field-effect transistors (TFETs) with gate-modulated Zener tunnel junctions at the source are regarded as prospective alternatives to metal-oxide-semiconductor field-effect transistors (MOSFETs). There was a large number of investigations published in recent years concerning the physical principles of tunneling mechanisms, architecture of devices, and optimization of device characteristics. It was shown that significant increases of the device performance are obtained by integration of smaller bandgap materials in the source of Si-based TFETs, or by applying heterostructures of group III-V materials allowing an additional tailored-made band alignment. Caused by the lattice misfit, however, a large amount of strain is induced in heterostructures which might cause the generation of defects such as dislocations. These defects may alter the device characteristics dramatically. On the other hand, dislocations represent native nanostructures with diameters of about 1 nm and outstanding properties [1]. The present paper deals for the first time with the effect of defined numbers and types of dislocations in the near intrinsic region of gated pin structures (TFETs) prepared on silicon-on-insulator (SOI) substrates. Silicon acts here as a model substance. Experimental data in combination with device simulations are presented showing the effect of dislocations on the tunneling current. Different gate- and drain-voltage dependent tunneling mechanisms are identified.

2. Device Preparation
Defined two-dimensional dislocation networks were realized in the middle of 60 nm thick silicon layers formed by hydrophobic wafer direct bonding of SOI wafers \(<100>\) orientation. The wafer bonding process and feasibilities to attain arrangements of different numbers and types of dislocations are described elsewhere [1]. TFETs were prepared on such substrates. The channel direction was oriented in one of the \(<100>\)-directions, i.e. parallel to the dislocations. Boron and arsenic implantations were applied to define highly doped source and drain regions. The gate stack consists of a SiO₂ layer (thickness 3 nm) and a 100 nm thick polycrystalline Si layer. All process steps are similar to those used for MOSFETs [1]. In order to identify the effect of dislocations on electrical parameters of TFETs, reference devices were prepared without dislocations.

3. Results
Most of the existing TFET models assume that the gate-source voltage \( V_{GS} \) alone determines the band bending in the source-channel region. In a recently published analytical model the drain-source voltage \( V_{DS} \) dependence was added, which determines the position of the Fermi level in the drain [2]. Therefore it is important to analyze the effect of \( V_{DS} \) and \( V_{GS} \) separately. The impact of \( V_{DS} \)

All diodes with and without dislocations show regions of negative differential resistance (NDR) in the forward-bias regime indicating band-to-band-tunneling (BTBT). The peak-to-valley current ratio (PVCR) is the largest for diodes without dislocations (see inset Fig. 1) and decreases if dislocations are present in the channel. A similar behavior was obtained also by other authors [3].

![Fig. 1 Temperature dependence of the diode current on the temperature for different source-drain voltages (VDS). The inset shows the I-V characteristics at room temperature. Measurements on diodes without dislocations (reference).](image-url)
Low-temperature measurements proved a $T^{3/2}$-dependence of the current for diodes without dislocations referring to Shockley-Read-Hall (SRH) recombination as the dominant mechanism. An analogous dependence of the current was not obtained for diodes with dislocations in the channel. There are also no indications of variable range hopping conduction (Mott processes) which require a $T^{1/2}$-dependence. Hopping processes were assumed for high defect levels in solar silicon. This suggests that individual dislocations (or small numbers of these defects as regarded here) result in one or only a few defect bands in the gap.

The impact of $V_{GS}$

Fig. 2 shows the transfer characteristics of nTFETs without and with different dislocations. Devices without dislocations (reference) possess low subthreshold swings of about 60 mV/dec as well as drain voltage ($V_{DS}$) depending threshold voltages. Both characterize these devices as TFETs. This is confirmed by device simulations. TFETs with dislocations show a different behavior. Larger subthreshold swings and significant shifts of the threshold voltage ($V_T$) are most remarkable. The physical reason behind these is that energy barrier narrowing is a complex function of both $V_{GS}$ and $V_{DS}$.

In order to explain the physical mechanisms, low-temperature measurements were carried up to 4 K. All devices show only small effects on $I_{DS}$ at $T < 100$ K suggesting that BTBT is the dominant process in this temperature region. Characteristic differences between devices with and without dislocations exist, however, at higher temperatures ($T > 100$ K). Besides BTBT, also trap-assisted tunneling mechanisms act even in the subthreshold region. Plots of $\ln(J/E)$ vs. reciprocal temperature result in straight lines for reference devices indicating the presence of Poole-Frenkel emission [4] (Fig. 3a). Here, $J$ means the current density ($A/cm^2$) and $E$ is the electric field ($V/cm$). Barrier heights $\Phi_B$ between 80 meV and 180 meV are calculated. It is assumed that the related defects are interface traps. On the other hand, different mechanisms act in the presence of dislocations. Instead of a dependence on the electric field, a dependence on the temperature exists. As shown in Fig. 3b, the experimental data are fitted by assuming thermionic emission [4]. Different barrier heights $\Phi_T$ are estimated for different dislocation types.

3. Conclusions

The impact of $V_{GS}$ and $V_{DS}$ on the tunnel current of TFETs was analyzed. The effect of $V_{DS}$ results in SRH recombination for devices without dislocations. The dependence on $V_{GS}$ is characterized by Poole-Frenkel emission on interface traps. On the other hand, BTBT in TFETs with dislocations is controlled by thermionic emission (dependence on $V_{GS}$). The dependence on $V_{DS}$ causes additional trap-assisted tunneling mechanisms showing a complex dependence not only on the temperature or electric field.

References