Enhanced Subthreshold Slope and On-state Current in Tunneling Thin-Film-Transistors Using Metal Induced Lateral Crystallization

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Abstract
In this study, we propose a tunneling TFT fabricated by MILC method for the first time. The MILC tunneling TFTs demonstrate a lower subthreshold swing, ~232 mV/dec, than the other tunneling TFTs (T-TFTs) and a high on/off ratio > 10^6 at V_{DS}=1V without any hydrogen related plasma treatment.

1. Introduction
Recently, TFETs are receiving considerable attention for their potential to replace conventional metal-oxide-semiconductor- field-effect transistors (MOSFETs) for future low power application [1-3]. While considerable attention has been focused on sc-Si TFETs [2-4], a literature on issues of polycrystalline-Si T-TFTs has emerged slowly at present and has only focused on the devices crystallized by excimer-laser annealing (ELA)[5, 6] or by sequential lateral solidification (SLS) growth technique [7].

To further improve the tunneling current and to obtain a steeper subthreshold slope of the devices, T-TFTs and conventional TFTs (C-TFTs) fabricated with MILC method on the same wafer were demonstrated and characterized in this paper.

2. Experimental Methods
The process flow of the T-TFT is shown in Fig. 1. A p-type Si wafer capped with a 550 nm wet oxide layer was used as a starting substrate. A 70-nm-thick amorphous-Si layer was deposited by low pressure chemical vapor deposition (LPCVD) at 500°C and crystallized with MILC method as the channel film. The active region was defined by an i-line stepper and patterned. A 200 nm SiO\textsubscript{2} dummy gate was formed, and tunneling TFTs were implanted using boron and phosphorous to a dose of 5×10\textsuperscript{15} cm\textsuperscript{-2} as source and drain, and were annealed at 600°C in N\textsubscript{2} ambient to activate the dopants after dummy gate removal. At the same time, a C-TFT was fabricated on the same wafer with only phosphorous doping. A 30 nm gate oxide was then deposited by electron-beam evaporation. Then, aluminum metallization was used as source/drain contact and gate electrode.

3. Results and Discussion
The transfer characteristics of 40 tunneling TFTs and 40 control TFTs (C-TFTs) are presented in Fig. 2. A significant improvement in off-state leakage was obtained because of the large barrier for field emission. It is worth noting that the on-state current of the T-TFTs is only an order lower than the C-TFTs and that the subthreshold slope of the T-TFTs steeper than that of the C-TFTs is first achieved. The comparisons of the device parameters for different T-TFTs [5-7] are listed in Table. I. Figure 3 (a) and (b) present the output characteristics of the C-TFTs and T-TFTs, respectively. Despite the fact that the drive current of tunneling FETs is generally much lower than MOSFETs owing to relatively low tunneling efficiency [8], the on-state current of the MILC T-TFTs is only an order lower because of the occurrence of trap assisted tunneling (TAT).

To find out the approach to further improve the subthreshold slope of the MILC T-TFTs, the activation energy and interface state density (N\textsubscript{it}) were measured. The activation energy was extracted at V_{D} = 0.1V and plotted against V_{G} in Fig. 4. Three different gate bias ranges can be distinguished corresponding to different transport mechanisms: Shockley-Read-Hall generation, TAT, and BTBT. The activation energy was around 0.55 eV in the negative gate bias region, indicating that Shockley-Read-Hall generation dominates [9]. An activation energy of 0.3-0.5 eV was extracted at the subthreshold region, which were commonly attributed to TAT and/or emission from traps [9]. Finally, as gate bias increased, BTBT began and resulted in an activation energy of only 0.10 eV [9].

The T-TFTs were subjected to NH\textsubscript{3} plasma treatment for 10 minutes, which is helpful to passivate dangling bonds and reduce the amount of interface states. According to the charge-pumping measurement, the N\textsubscript{it} of the T-TFTs (W/L=10μm/5μm) can be suppressed from 1.22×10\textsuperscript{11} cm\textsuperscript{-2} to 9.22×10\textsuperscript{10} cm\textsuperscript{-2} (Fig. 5). Both the subthreshold slope and the on/off ratio are improved after plasma treatment as shown in Fig. 6. As a result, minimizing the occurrence of TAT and the amount of N\textsubscript{it} would be an essential issue to achieve sub-60 mV/dec for T-TFTs.

The dependence of the on/off current on the channel length can be seen in Fig. 7. The drive current and off-leakage of T-TFTs are nearly independent indicating that a large on/off ratio can be well sustained even after length scaling.

3. Conclusions
In conclusion, poly-Si tunneling TFTs have been fabricated and characterized successfully for the first time. The tunneling TFTs with MILC channels show high tunneling current, low off-leakage, steep subthreshold swing, and...
large on/off ratio. These devices will be suitable for the application in low standby power circuits, as drivers of AMLCDs, and as three-dimensional integrated circuits in the future.

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References

Table I  Comparison of Several Important Parameters of The Tunneling TFTs With Previous Studies.

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<tr>
<td>Channel Length (μm)</td>
<td>10</td>
<td>10</td>
<td>0.2</td>
<td>1</td>
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<tr>
<td>Channel Film Thickness (μm)</td>
<td>70</td>
<td>70</td>
<td>100</td>
<td>20</td>
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<td>Average S.S. (mV/dec)</td>
<td>232</td>
<td>297</td>
<td>&gt; 2500</td>
<td>~ 400</td>
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<td>Layer (μA/μm²)</td>
<td>0.59</td>
<td>1.82</td>
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<td>&lt; 0.1</td>
</tr>
<tr>
<td>On-Off Ratio</td>
<td>6.3 × 10⁶</td>
<td>3.6 × 10⁶</td>
<td>&gt; 10⁶</td>
<td>&gt; 10³</td>
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Fig. 1 Key process flows of the tunneling TFTs.

Fig. 2 Transfer characteristics of tunneling TFTs and control TFTs.

Fig. 3 Output characteristics of (a) tunneling TFTs and (b) control TFTs.

Fig. 4 Activation energy of the tunneling TFT versus the gate bias.

Fig. 5 The on/off ratio and subthreshold slope comparisons between T-TFTs before and after plasma treatment at V_D = 1V. The channel length/width is 10/10 μm.

Fig. 6 The T-TFT charge pumping current as a function of frequency before and after plasma treatment.

Fig. 7 The T-TFTs on/off current as a function of the gate length at V_D = 0.1V. The channel width is 10 μm.