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Layout Design Considering Electro-thermal Properties for CMOS Inverter Composed of Multi-pillar Vertical MOSFET

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Abstract

In order to attain high-speed circuits, CMOS inverter composed of multi-pillar (2 pillar NMOS and 4 pillar PMOS) 22nm feature size vertical MOSFET is numerically studied considering electro-thermal properties by 3-D device simulation. It is shown that the linear type layout (NMOS: 1x2, PMOS: 1x4) shows higher heat dissipation efficiency compared to the square type layout (NMOS: 2x1, PMOS: 2x2), because twice numbers of gate contacts in linear type layout compared to the square type layout perform as excellent heat sinks. Furthermore, we evaluate the impact of self-heating effect toward voltage transfer characteristics of CMOS inverter.

1. Introduction

With Very Large Scale Integration (VLSI) density increasing, self-heating effect becomes a crucial problem, which degrades the performance of the circuit [1]. Therefore, it is clear that layout design needs to consider not only electrical properties but thermal properties as well. In order to overcome the self-heating problem in the VLSI, high efficient heat dissipation layout is desired. On the other hand, multi-pillar vertical MOSFET attracts broad attention as the platform of future VLSI for its excellent device performance [2, 3]. In previous research, the compact and high electrical performance of layout design for multi-pillar vertical MOSFET has been investigated [2, 3]. However, the compact layout prevents the heat dissipating, which will degrade the electrical performance of the circuits.

In this paper, we present the effect of self-heating effect to layout design of CMOS inverter composed of multi-pillar vertical MOSFET.

2. Simulation Settings

Figure 1 shows the structure of vertical MOSFET [4, 5]. Figure 2 shows the simulated layout patterns of CMOS inverter composed of multi-pillar vertical MOSFET. Here, 2 pillar NMOS and 4 pillar PMOS compose one CMOS inverter cell. Table I shows the parameters for the simulation. As thermal boundary, we assumed the case that that all adjacent cells are active. Particularly, thermal resistance equivalent to 50um Si substrate is attached below the simulation area and 12 layers of interconnect are attached above the simulation area (M1 Metal). In previous studies, the hot spot of CMOS inverter composed of vertical MOSFET is shown at the NMOS drain side [6] and GND is shown to perform as a better heat sink compared to VDD [7]. In order to restrain calculation load, depletion type of MOSFET is adopted to simulate non-isothermal simulation for assessing the electro-thermal properties.

3. Results and discussions

Figure 3 shows the power due to DC through current and Fig.4 shows the lattice temperature distribution for different layout patterns under maximum input power. Figure 5 (a), Fig.6 (a) shows the cross-sectional view of each layout. First, the NMOS Si pillar next to the NMOS bottom source contact shows the highest temperature as from Fig.5 (b). Due to lower bottom source resistance, larger electric current flows in the pillar next to the source contact as from Fig.5 (c), leading larger joule heating, while the pillar with same distance from source contact shows the same current density as from Fig.6 (c). Second, the NMOS Si pillar apart from the NMOS gate contact shows the highest temperature from Fig.6 (b). Besides, the linear type (NMOS: 1x2, PMOS: 1x4) shows lower temperature compared to the square type (NMOS: 2x1, PMOS: 2x2). This is due to twice numbers of gate contacts around NMOS, performing as good heat sinks, in the linear type compared to the square type as shown in Fig.7. We evaluated the heat dissipation efficiency by thermal resistance (R_{th}) of the layout structures as shown in Fig.8. As from Fig.8, the NMOS linear type shows higher heat dissipation. (78% Rth of square type layout) Here, common-gate layout shows higher heat dissipation efficiency than separate-gate layout because the heat can dissipate from hot spot (NMOS drain side) easily. Moreover, we investigated the self-heating effect toward the voltage transfer characteristics for different layout patterns by using 3-D device isothermal simulation as shown in Fig.9. In Fig.9, the negative effect of self-heating effect to electrical performance is shown. Because of higher temperature, the square type shows severer performance degradation compared to the linear type.

4. Conclusions

CMOS inverter composed of multi-pillar (2 pillar NMOS and 4 pillar PMOS) 22nm feature size vertical MOSFET is numerically studied considering electro-thermal properties by 3-D device simulation. It is shown that the linear type layout (NMOS: 1x2, PMOS: 1x4) shows higher heat dissipation efficiency compared to the square type layout (NMOS: 2x1, PMOS: 2x2), because twice numbers of gate contacts, performing as excellent heat sinks, in linear type layout compared to the square type layout. Besides, the linear type layout shows less impact of self-heating effect toward voltage transfer characteristics of CMOS inverter compared to the square type layout.

Acknowledgements

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References

[1] O. Semenov *et al.*, IEEE Transactions on vol.6, no.1, pp.17, 27, (2006).
[2] Y. Norifusa *et al.*, IMFEDK Dig. Tech., pp. 27-28, (2008).
[3] K. Sakui *et al.*, IEEE Transactions on , vol.57, no.8, pp.1768,1773, (2010).
[4] T. Endoh *et al.*, IEICE Trans. on Electronics, Vol.E80-C, No.7, pp.911-917, (1997).
[5] T. Endoh *et al.*, IEICE Trans. Electron, 108, 122, 101-105, (2008)
[6] A. Wang *et al.*, IWCE(2013) *accepted.*
[7] A. Wang *et al.*, AWAD(2013) *accepted.*

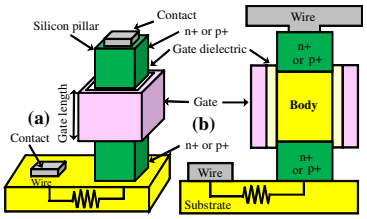


Fig. 1 Structures of vertical MOSFET.

Table I Parameters

Feature Size (*F*)	22nm
Pillar Diameter (*Dp*)	*F* (=22nm)
Gate Length (*Lg*)	2*F* (=44nm)
Gate Oxide Thickness (*tox*)	1.2nm
STI thickness (*tsti*)	300nm
Ambient Temperature (*Tamb*)	400K
Power Supply (*Vdd*)	0.9V

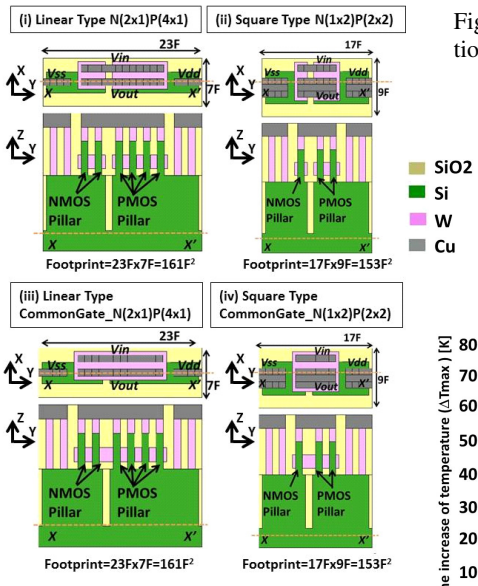


Fig. 2 The simulated layout of CMOS inverter of multi-pillar vertical MOSFET.

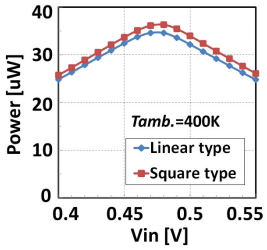


Fig. 3 Power for (i) Linear type, (ii) Square type.

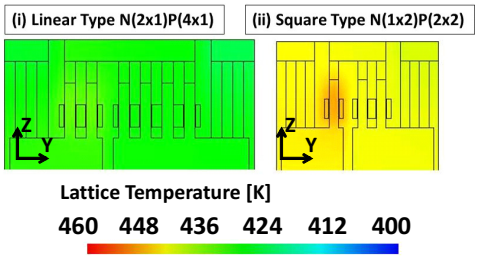


Fig. 4 Lattice temperature distribution for different layout patterns.

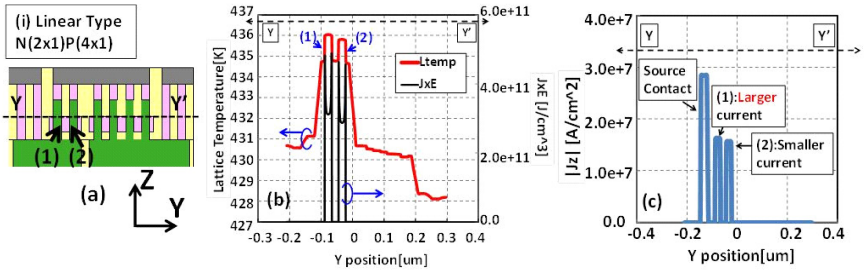


Fig.5 (a) Linear type layout cross-sectional view and (b) the lattice temperature distribution and joule heating, (c) current density for a cross-section line of NMOS drain side.

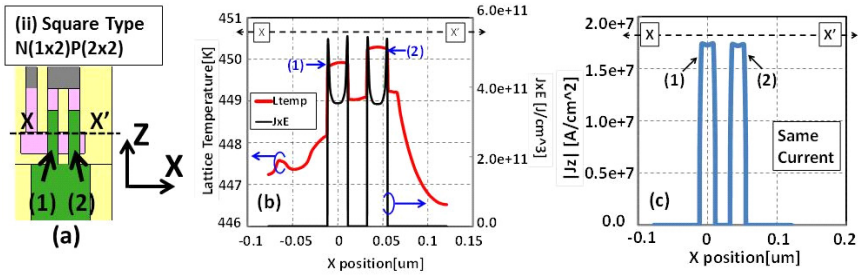


Fig.6 (a) Square type layout cross-sectional view and (b) the lattice temperature distribution and joule heating, (c) current density for a cross-section line of NMOS drain side.

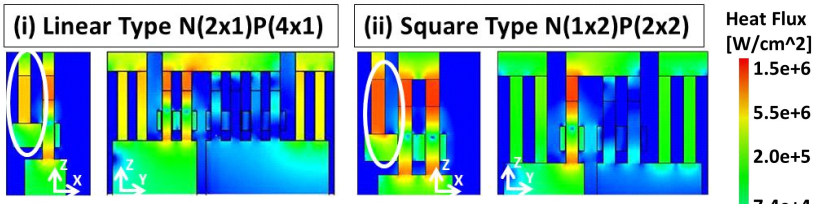


Fig.7 Heat flux distribution for different layout structures. Gate contact shows great performance as a heat sink.

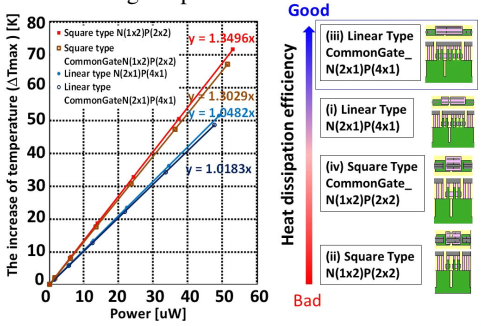
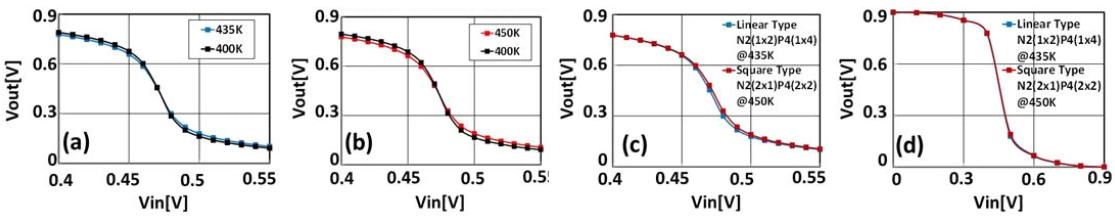


Fig.8 Thermal resistance (R_{th}) of the layout structures. Linear type layout shows higher heat dissipation efficiency compared to the square type layout. Here, the increase of temperature is the difference between the peak temperature and the ambient temperature (=400K).



(a) linear type (b) square type (c) comparison (d) comparison (a complete view)

Fig.9 Self-heating effect to the voltage transfer characteristics for the linear type layout and the square type layout.