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Negative differential conductivity in Gate-All-Around Si Nanowire FETs and its impact on Circuit Performance

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Abstract

A fully-coupled continuum based 3-D numerical analysis is performed to understand the device-circuit co-optimization issues due to device self-heating and carrier heating effects in Si Gate All-Around (GAA) Nanowire Field Effect Transistors (NWFETs). Employing coupled 3-moment based Energy Transport (ET) formulations and Quantum Confinement (QC) effect; we report the evidence of Negative Differential Conductivity (NDC) in NWFETs and its effect on signal propagation delay in NWFET based CMOS inverter and 3-stage Ring Oscillator (RO) circuits.

1. Introduction

The carrier transport in thin Si-NWFET is dictated by strong 2-D QC (QC: Spatial and Electrostatic confinement) with 1-D degree of freedom in carrier momentum. The 2-D QC in thin nanowire body affects the electronic and phonon energy dispersions. These effects enable GAA Si NWFETs to have superior electrostatic integrity, improved short channel performance and high I_{ON} to I_{OFF} ratio at constant supply voltage. But the reduced lattice thermal conductivity, quasi 1-D heat flow and higher thermal contact resistance makes NWFETs susceptible to higher Self-Heating Effect (SHE) [1]. Increased SHE degrades phonon limited carrier mobility, thus reducing I_{ON} and also causing negative differential conductance effect in output characteristics. This also changes carrier energy relaxation rates (increasing hot carrier population) and increases I_{OFF}. Such SHE has already been experimentally shown in Si GAA NWFETs [2] and metallic carbon nanotubes [1]. In this work, we present 3D numerical simulations on device and logic circuit performance of GAA Si-NWFETs considering 2D QC and SHE.

2. Device Structure and Simulation Framework

The short-channel GAA Si NWFET structure considered in the simulation study and schematic of quasi 1-D heat transport along the nanowire body are shown in Fig. 1 (a). The NWFET structures are optimized for sub-22nm generation logic technologies. Various NW diameters (21.4nm-7nm), L_{gate} (35nm-14nm), $T_{OX,E}$ (1.5nm-0.9nm), heavy Source/Drain doping (~10^{20}cm^{-3}), $N_{Channel}$ (~10^{15}cm^{-3}) are considered with I_{OFF} (~1nA/μm). The computed electronic band structure of a 7nm thick cylindrical Si NW along [100] direction using the tight binding methodology program [3] is shown in Fig 1 (b). Energy band-gap (E_G) variation due to quantum size effects and lower lattice thermal conductivity values, with dirichlet thermal boundary conditions, are considered in the numerical study. The coupled system of device equations are solved in a self-consistent iterative scheme for both device and mixed-mode (MM) simulations [4]. The carrier mobility model parameters with quantum correction of inversion charge for Drift-Diffusion (DD) transport are calibrated with measured NWFET data [5]. The hardware calibrated NWFET transfer characteristics are shown Fig. 2.

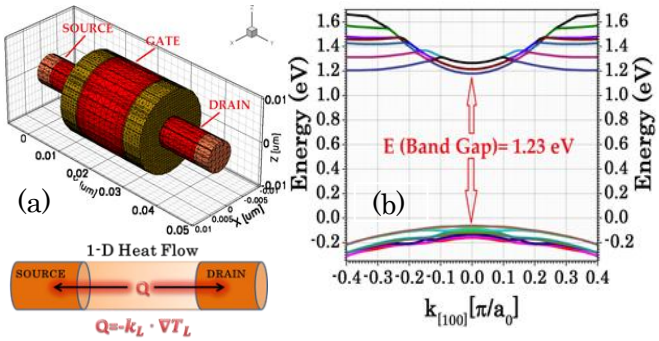

Fig. 1 (a) Si Nanowire FET 3D structure and Schematic of quasi 1-D heat flow in NWFET, (b) Computed electronic energy band structure of 7nm diameter Si nanowire.

3. Results and Discussion

Fig. 3 shows the quantum corrected inversion charge density spatial profile in the Si-nanowire body. The thinner nanowire (d=7 nm) enables volume inversion operation due to strong 2-D QC. The improved electrostatic control of the gate over channel in GAA NWFET is shown in Fig. 4, where, the sub-threshold I_d-V_{gs} for nFET and pFET are compared with recently introduced Tri-Gate FETs by Intel [6]. The GAA NWFET experiences lower short channel effects

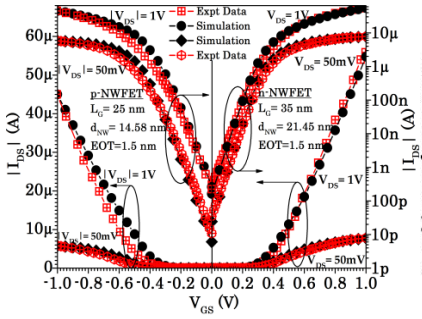

Fig. 2 Calibrated NWFET transfer Characteristics with Expt. Data [5].

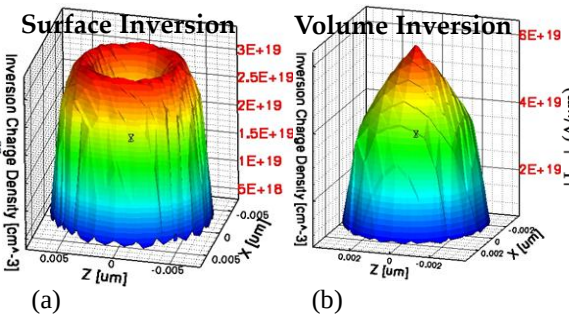

Fig. 3 Quantum corrected inversion charge density in n-NWFET for (a) 14nm and (b) 7nm diameter wires.

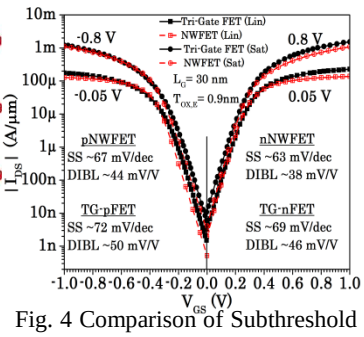

Fig. 4 Comparison of Subthreshold I_d-V_{gs} of GAA NWFETs with Tri-gate FETs of Intel [6].

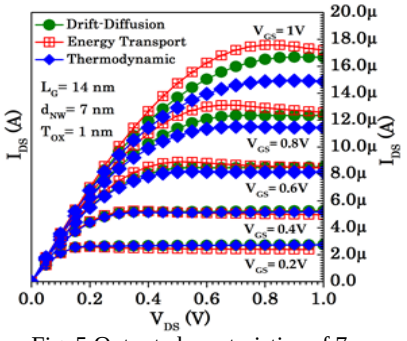

Fig. 5 Output characteristics of 7 nm diameter n-NWFET.

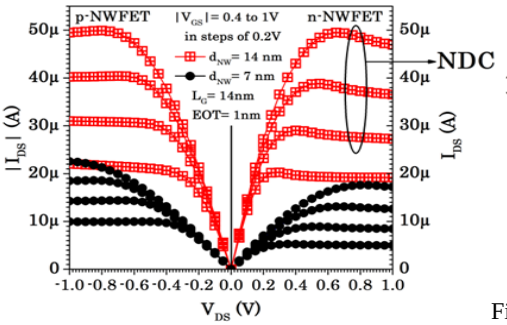

Fig. 6 n-NWFET and p-NWFET output characteristics from energy transport simulations.

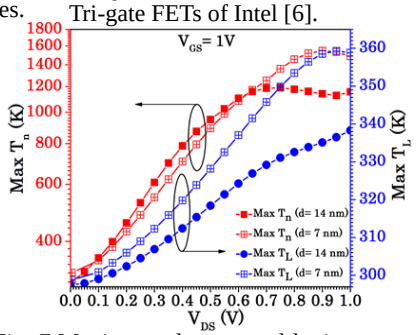

Fig. 7 Maximum electron and lattice temperature in n-NWFET for different drain bias at V_{GS}= 1V.

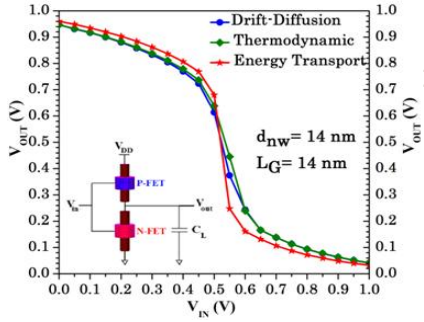

Fig. 8 Si NWFET based CMOS inverter voltage transfer characterstics for different transport models.

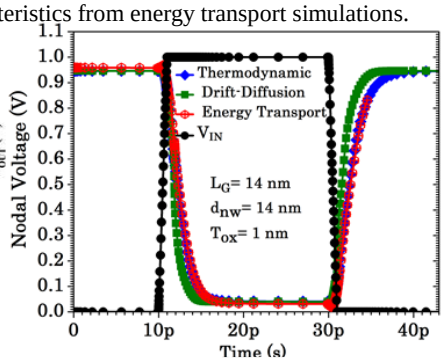

Fig. 9 Si NWFET based inverter pulse response for different transport models.

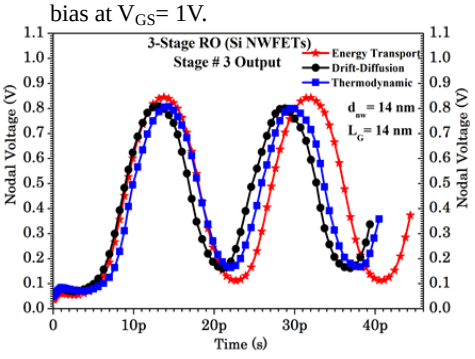

Fig. 10 FO1 3-stage RO nodal output voltage swing for different transport models.

with steeper sub-threshold slopes (~9% steeper) and lower Drain Induced Barrier Lowering (DIBL) (~17% lower) compared to tri-gate FETs [6]. The output characteristics of the n-FET (d= 7nm), for different transport models, are compared in Fig. 5. The self-heating effect is clearly visible in the n-FET output characteristics with NDC signatures, obtained by energy-transport simulations. Similar SHE is observed for n- and p-FETs (d=14nm) as shown in Fig. 6. In Fig.7, the thinner NWFET (d=7nm) shows 28% higher carrier heating and 6% higher lattice heating than the NWFET (d=14 nm) at V_{GS}=V_{DS}=1 V due to SHE.

In the transient mixed-mode simulations, for a NWFET (d=14 nm) based CMOS inverter (Fig. 8), about 59% higher signal propagation delay is predicted by the ET model compared to DD transport as shown in Fig. 9. The Si GAA NWFET based FO-1 3-Stage RO output signal frequency is found to be lower by 11% as predicted by ET model compared to the DD transport ($f_{osc} = 62.93\ GHz$), due to the combined effects of carrier heating and SHE as shown in Fig. 10.

4. Conclusions

These 3-D numerical studies demonstrate that GAA Si NWFETSs have excellent electrostatic integrity due to strong 2D quantum confinement. The thin GAA device geometry affects carrier dynamics and lattice heat flow leading to hot carrier and self-heating effects. The impact of negative differential conductivity on CMOS inverter and 3-stage ring oscillator circuits is analyzed and it is shown that the self-heating effects can contribute to over 50% higher propagation delay in GAA NWFET circuits. This emphasizes the need for device-circuit co-optimization for GAA nanowire based devices.

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