Negative differential conductivity in Gate-All-Around Si Nanowire FETs and its impact on Circuit Performance

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Abstract

A fully-coupled continuum based 3-D numerical analysis is performed to understand the device-circuit co-optimization issues due to device self-heating and carrier heating effects in Si Gate All-Around (GAA) Nanowire Field Effect Transistors (NW FETs). Employing coupled 3-moment based Energy Transport (ET) formulations and Quantum Confinement (QC) effect, we report the evidence of Negative Differential Conductivity (NDC) in NW FETs and its effect on signal propagation delay in NW FET based CMOS inverter and 3-stage Ring Oscillator (RO) circuits.

1. Introduction

The carrier transport in thin Si-NWFET is dictated by strong 2-D QC (QC: Spatial and Electrostatic confinement) with 1-D degree of freedom in carrier momentum. The 2-D QC in thin nanowire body affects the electronic and phonon energy dispersions. These effects enable GAA Si NW FETs to have superior electrostatic integrity, improved short channel performance and high \(I_{ON}\) to \(I_{OFF}\) ratio at constant supply voltage. But the reduced lattice thermal conductivity, quasi 1-D heat flow and higher thermal contact resistance makes NW FETs susceptible to higher Self-Heating Effect (SHE) \([1]\). Increased SHE degrades phonon limited carrier mobility, thus reducing \(I_{ON}\) and also causing negative differential conductance effect in output characteristics. This also changes carrier energy relaxation rates (increasing hot carrier population) and increases \(I_{OFF}\). Such SHE has already been experimentally shown in Si GAA NW FETs \([2]\) and metallic carbon nanotubes \([1]\). In this work, we present 3D numerical simulations on device and logic circuit performance of GAA Si-NWFETs considering 2D QC and SHE.

2. Device Structure and Simulation Framework

The short-channel GAA Si NW FET structure considered in the simulation study and schematic of quasi 1-D heat transport along the nanowire body are shown in Fig. 1 (a).

The NW FET structures are optimized for sub-22nm generation logic technologies. Various NW diameters (21.4nm-7nm), \(L_{gate}\) (35nm-14nm), \(T_{OX,E}\) (1.5nm-0.9nm), heavy Source/Drain doping (\(\sim 10^{20}\) cm\(^{-3}\)), \(N_{Channel}\) (\(\sim 10^{15}\) cm\(^{-3}\)) are considered with \(I_{OFF}\) (\(\sim 1nA/\mu m\)). The computed electronic band structure of a 7nm thick cylindrical Si NW along \([100]\) direction using the tight binding methodology program \([3]\) is shown in Fig 1 (b). Energy band-gap (\(E_{G}\)) variation due to quantum size effects and lower lattice thermal conductivity values, with dirichlet thermal boundary conditions, are considered in the numerical study. The coupled system of device equations are solved in a self-consistent iterative scheme for both device and mixed-mode (MM) simulations \([4]\). The carrier mobility model parameters with quantum correction of inversion charge for Drift-Diffusion (DD) transport are calibrated with measured NW FET data \([5]\). The hardware calibrated NW FET transfer characteristics are shown Fig. 2.

![Fig. 1 (a) Si Nanowire FET 3D structure and Schematic of quasi 1-D heat flow in NWFET. (b) Computed electronic energy band structure of 7nm diameter Si nanowire.](image)

3. Results and Discussion

Fig. 3 shows the quantum corrected inversion charge density spatial profile in the Si-nanowire body. The thinner nanowire (d=7 nm) enables volume inversion operation due to strong 2-D QC. The improved electrostatic control of the gate over channel in GAA NW FET is shown in Fig. 4, where, the sub-threshold \(I_{GS}-V_{GS}\) for nFET and pFET are compared with recently introduced Tri-Gate FETs by Intel \([6]\). The GAA NW FET experiences lower short channel effects
with steeper sub-threshold slopes (~9% steeper) and lower Drain Induced Barrier Lowering (DIBL) (~17% lower) compared to tri-gate FETs [6]. The output characteristics of the n-FET (d= 7nm), for different transport models, are compared in Fig. 5. The self-heating effect is clearly visible in the n-FET output characteristics with NDC signatures, obtained by energy-transport simulations. Similar SHE is observed for n- and p-FETs (d=14nm) as shown in Fig. 6. In Fig. 7, the thinner NW-FET (d=7nm) shows 28% higher carrier heating and 6% higher lattice heating than the NW-FET (d=14nm) at V_GS=V_D=1 V due to SHE.

In the transient mixed-mode simulations, for a NW-FET (d=14 nm) based CMOS inverter (Fig. 8), about 59% higher signal propagation delay is predicted by the ET model compared to DD transport as shown in Fig. 9. The Si GAA NW-FET based FO-1 3-Stage RO output signal frequency is found to be lower by 11% as predicted by ET model compared to the DD transport (f_puc = 62.93 GHz), due to the combined effects of carrier heating and SHE as shown in Fig. 10.

4. Conclusions

These 3-D numerical studies demonstrate that GAA Si NW-FETs have excellent electrostatic integrity due to strong 2D quantum confinement. The thin GAA device geometry affects carrier dynamics and lattice heat flow leading to hot carrier and self-heating effects. The impact of negative differential conductivity on CMOS inverter and 3-stage ring oscillator circuits is analyzed and it is shown that the self-heating effects can contribute to over 50% higher propagation delay in GAA NW-FET circuits. This emphasizes the need for device-circuit co-optimization for GAA nanowire based devices.

References