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Ge N-channel Omega-Gate Field Effect Transistors with [010] Channel Direction

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Abstract

We report Ge n-channel Omega-gate (Ω-gate) MOSFET with [010] channel direction and providing immunity against short channel effect even channel length down to 80 nm. The electrical characteristics with subthreshold swing of 136 mV/dec, DIBL of 56 mV/V, and the I_{ON}/I_{OFF} ratio 2×10^5 are presented.

1. Introduction

Ge has been regarded as a promising potential channel material to substitute Si channel for sub-14 nm CMOS technology. Because of better electrostatics, non-planar structure is very attractive for suppressing short channel effect of transistor in such small dimension [1]. High mobility Ge n-channel multiple-gate MOSFETs with [110] channel direction have ever been demonstrated, which can be easy to be integrated in the Si platform [2-3]. However, the performance of [010] channel direction non-planar Ge n-MOSFET has not been observed yet. In this work, Ge n-channel Ω-gate MOSFET with [010] channel direction have been demonstrated for the first time. We find Ω-gate structure is beneficial in alleviating short channel effects (SCE).

2. Experiment

The Si on insulator (SOI) substrate (10-20 ohm-cm) was trimmed down to ~20 nm by wet oxidation. A ~60 nm Ge film was grown by ultra high vacuum chemical vapor deposition (UHVCVD) system. A detail growth procedure can be referred to our previous study [3].

We fabricated our device using gate-last process because it is suitable for high-κ/metal gate stack. Fig. 1(a) shows a schematic view of non-planar Ge multiple-gate MOSFET. Phosphorus implants (20 keV, 1×10^{15} cm^{-2}) were used for source and drain doping after the [010] direction pattern was defined. The illustrative device layout is shown in Fig. 1(b). Dopant activation was performed and Ge fin was formed by using reactive ion etching (RIE) anisotropic etching. We performed a wet trimming process without causing additional damage for shrinking Ge fin width (W_{Fin}) down to ~30 nm by dilute H_2O_2. Buried oxide was etched by BOE to form a Ω-shape Ge fin as shown in Fig. 1(c). These are two key processes for scaling down the device dimension and Ω-gate formation. The GeO_2 surface passivation and ALD Al_2O_3 high-κ dielectric deposition was carried out. Finally, metal gate Ti (5 nm)/Pt (100 nm) was deposited by sputtering followed by metallization. The [010] channel direction Ge Ω-gate n-MOSFET devices with different mask channel lengths (L_{Mask}) from 1 μm to 80 nm were fabricated.

3. Results and Discussion

Fig. 2(a) and (b) show the cross-sectional TEM and magnified images of Ge (W_{Fin}~ 30 nm) Ω-gate MOSFET with GeO_2 (~2 nm)/Al_2O_3 (~5 nm) and Ti/Pt metal gate stack. Fig. 2(c) shows low defect dislocation of Ge/Si lattice interface image. Fig. 3 shows the I_{DS}-V_G transfer characteristic of Ge n-channel Ω-gate MOSFET with L_{Mask} of 80 nm and W_{Fin} of 30 nm. The subthreshold swing (S.S.) value is 136 mV/dec and the DIBL value is 56 mV/V. We can see I_{ON}/I_{OFF} ratio is ~2×10^5, which is one order of magnitude higher than that of the transistor with [110] channel in the previous report [2]. The I_{DS}-V_{DS} output characteristic is illustrated in Fig. 4.

To demonstrate the gate control ability of the short channel devices with Ω-gate structure, S.S. and DIBL as a function of L_{Mask} with W_{Fin} of 30 nm are shown in Fig. 5. We can see the devices depict excellent subthreshold characteristics which is better than those in our previous study [3] even L_{Mask} down to 80 nm. We think excellent subthreshold characteristics are attributed to the Ω-gate structure. Fig. 6 shows transconductance (g_m) and I_{ON}/I_{OFF} ratio as a function of L_{Mask} with W_{Fin} of 30 nm. The devices with shorter channel length possess higher g_m and enhanced I_{ON}/I_{OFF} ratio. Fig. 7 shows S.S. and DIBL as a function of W_{Fin} with L_{Mask} of 80 nm. We can see that swing and DIBL are controlled tightly by narrower W_{Fin} devices in the short channel region. Furthermore, a high performance device can be achieved by simple process. Hence, short channel [010] Ge n-channel Ω-gate MOSFET with high performance has been demonstrated successfully.

4. Conclusions

Ge n-channel Ω-gate MOSFETs with [010] channel direction and high-κ/metal gate stack integrated in the Si platform have been fabricated for the first time. The device with L_{Mask}= 80 nm (W_{Fin}=30 nm) depict S.S.=136 mV/dec, DIBL=56 mV/V and I_{ON}/I_{OFF}= 2×10^5; Ω-gate structure is able to effectively suppress the short channel effects.

Acknowledgements

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5. Reference

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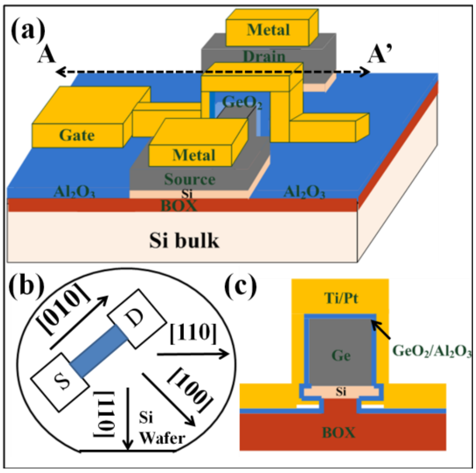

Fig. 1 (a) Schematic view of Ge multiple-gate MOSFET with high-κ/metal gate stack. (b) Schematic illustration of device layout on (100) Si wafer. (c) Ω-shape Ge fin along A-A'.

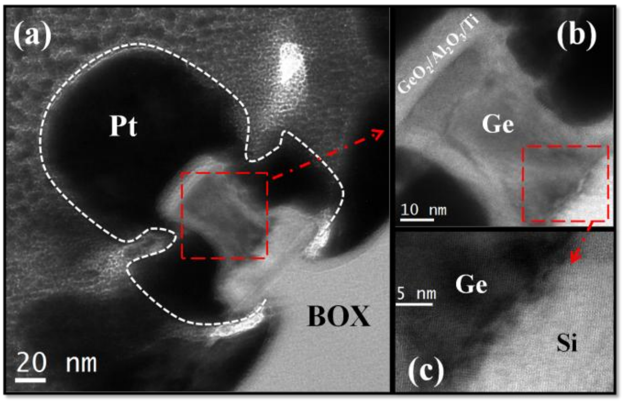

Fig. 2 (a) and (b) show the cross-sectional TEM images of Ge Ω-gate MOSFET. (c) Ge/Si lattice interface image.

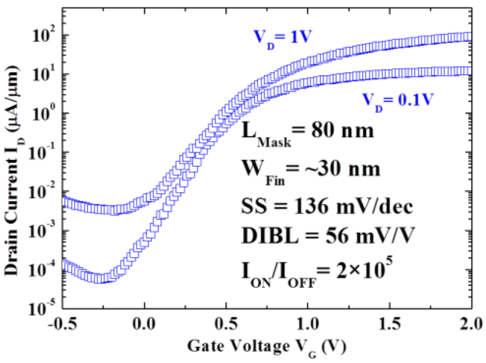

Fig. 3 I_{DS} - V_G transfer characteristic of Ge n-channel Ω-gate MOSFET with L_{Mask} of 80 nm and W_{Fin} of 30 nm.

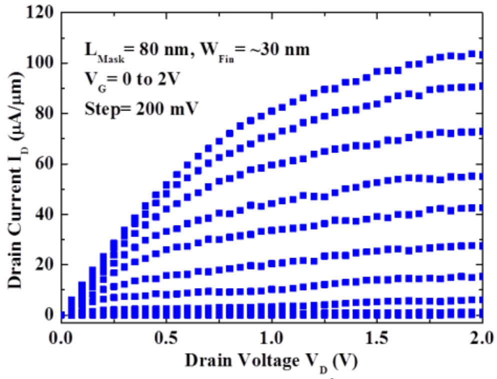

Fig. 4 I_{DS}-V_{DS} output characteristic of Ge n-channel Ω-gate MOSFET with L_{Mask} of 80 nm and W_{Fin} of 30 nm.

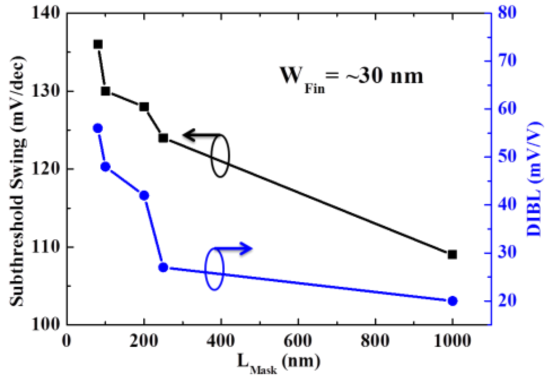

Fig. 5 S.S. and DIBL of Ge n-channel Ω-gate MOSFET with W_{Fin} of 30 nm versus L_{Mask} of 80-1000 nm.

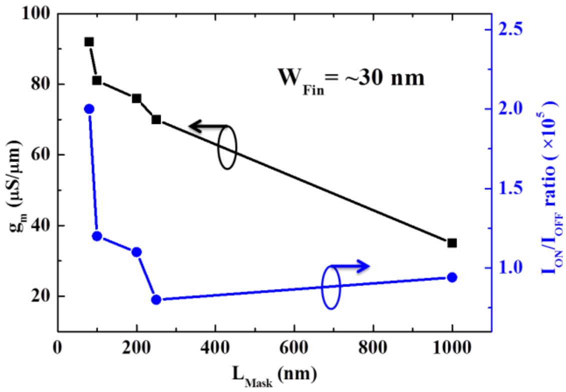

Fig. 6 g_m and I_{ON}/I_{OFF} ratio of Ge n-channel Ω-gate MOSFET with W_{Fin} of 30 nm versus L_{Mask} of 80-1000 nm.

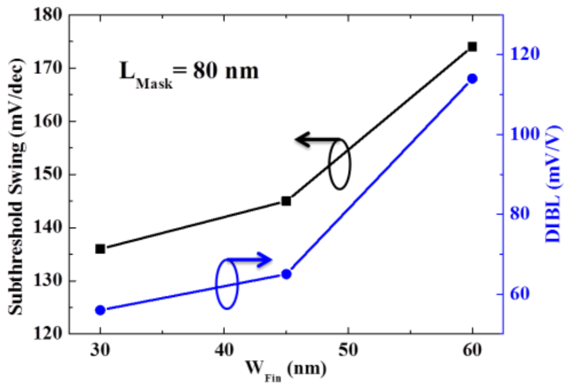

Fig. 7 S.S. and DIBL of Ge n-channel Ω-gate MOSFET with L_{Mask} of 80 nm versus W_{Fin} of 30-60 nm.