Effects of Rutile TiO$_2$ Interlayer on HfO$_2$/Ge MOS Structure

K. Kobashi$^{1,2}$, T. Nagata$^2$, T. Nabatame$^2$, Y. Yamashita$^2$, A. Ogura$^1$, and T. Chikyow$^2$

$^1$ Nanotechnology Laboratory, Meiji University, 1-1-1 Higashimita, Tama-ku, Kawasaki, Kanagawa 214-8571, Japan
$^2$ Nano-Electronics Materials Unit, International Center for Materials Nanoarchitectonics (WPI-MANA), National Institute for Materials Science, 1-1 Namiki Tsukuba, Ibaraki 305-0044, Japan
Phone: +81-29-860-4725 E-mail: CHIKYO.Toyohiro@nims.go.jp

Abstract

The rutile TiO$_2$ interlayer is inserted between HfO$_2$ and Ge to passivate a Ge surface. XPS results show that the GeO$_x$ formation was effectively suppressed. capacitance–voltage characteristic shows EOT = 0.84 nm and small hysteresis. These results suggest the Ge surface passivation utilizing the rutile TiO$_2$ interlayer is promising for the future Ge MOS devices.

1. Introduction

As a result of aggressive scaling of CMOS devices, the Si channel is approaching a scaling limit. Ge channel has been attracted much attention because of high electron and hole mobility, which lead to higher drive current, compared to those of Si [1,2]. Furthermore, narrower band gap of Ge than that of Si allows the supply voltage scaling [3]. However, Ge based CMOS devices still have problems to be solved. One of the critical problems is high defect densities at the interface between high-k and Ge [4].

For this problem, there are many studies to passivate Ge surface such as GeN (GeON) passivation [5,6], Si passivation [7] and F passivation [8]. Among those studies, the Ge surface nitridation technique has been shown to reduce hysteresis and leakage current so far. However, nitride layer such as GeN or GeON has low dielectric constant, which prevents further device scaling for future logic device. In this study, a TiO$_2$ interlayer was investigated as a passivation layer between HfO$_2$ and Ge. Due to the low heats of formation value for TiO$_2$ compared to that for GeO$_2$, TiO$_2$ might suppress the formation of defective GeO$_x$, which is one of the causes of poor electrical properties [9]. In addition, rutile TiO$_2$ has much higher dielectric constant ($k = 80$) [10] than the nitrided film, which enables further device scaling.

2. Experiment

The starting wafers were p-Ge (100) wafers with a resistivity of 0.01-0.05 $\Omega$ cm. The native oxide (GeO$_x$) was removed by annealing at 420 °C for 10 min in an ultra high vacuum (UHV) chamber. After that, a 6 nm-thick-TiO$_2$ film was deposited on the Ge substrate by pulsed laser deposition (PLD) with a KrF excimer laser ($\lambda = 248$ nm) at a substrate temperature of 450 °C below a vacuum level of 6.7 x 10$^{-5}$ Pa, followed by 6 nm-thick-HfO$_2$ deposition at a substrate temperature of 300 °C in oxygen partial pressure of 1.3 x 10$^{-4}$ Pa. In these depositions, laser energy density and laser frequency were set as 1.0 J/cm$^2$ and 5 Hz, respectively. After the film deposition, rapid thermal annealing (RTA) was performed in N$_2$ ambient at 300 °C for 5 minutes. To measure electrical property, a 160 nm-thick-Pt gate electrode with a diameter of 100 μm was deposited on the HfO$_2$/TiO$_2$/Ge structure by DC-magnetron sputtering. Finally, forming gas annealing (FGA, 96 %N$_2$ + 4%H$_2$) was performed at 300 °C for 30 minutes. The crystal structures of the TiO$_2$ films were identified by x-ray diffraction (XRD: Bruker axs, D8 Discover Super Speed) measurement with Cu Ka radiation and reflection high-energy electron diffraction (RHEED). To examine interfacial reaction between the TiO$_2$ film and the Ge substrate, chemical bonding states were determined by x-ray photoelectron spectroscopy (XPS: Thermo Scientific, VG Theta Probe) with a monochromatic Al Ka radiation x-ray source ($hv = 1486.6$ eV). For electrical property, capacitance–voltage (C-V) and current–voltage (I-V) characteristics were measured by a semiconductor parametric analyzer (Agilent, B1500A).

3. Results and discussion

Figure 1 shows RHEED patterns taken from the [010] azimuth for the Ge (100) surface (a) before and (b) after annealed at 420 °C for 10 min in UHV. After annealing, the Ge (100) surface shows streak patterns accompanied with Kikuchi lines, meaning that GeO$_x$ was removed and a clean Ge surface was obtained.

![RHEED pattern for the Ge (100) surface (a) before and (b) after annealed at 420 °C for 10 min in UHV.]

Fig. 1 RHEED pattern for the Ge (100) surface (a) before and (b) after annealed at 420 °C for 10 min in UHV.

RHEED and XRD patterns of the TiO$_2$ film deposited on the Ge substrate at various substrate temperatures are shown in Fig. 2. Halo patterns in RHEED and no XRD pattern corresponding to TiO$_2$ were observed at a substrate temperature of 300 °C, indicating that the TiO$_2$ layer is amorphous structure. In contrast, a streak pattern attributed to rutile TiO$_2$ began to appear when the TiO$_2$ film was deposited at a substrate temperature of 450 °C, which was consistent with XRD patterns. The peak intensity of rutile (200) in the XRD patterns increased when TiO$_2$ was deposited at a substrate temperature of 600 °C, suggesting that the crystallinity of TiO$_2$ film improved.
Fig. 2 RHEED and XRD pattern of TiO$_2$ deposited at different substrate temperature.

However, XPS measurements revealed that the high substrate temperature process caused the interface reaction between the TiO$_2$ film and the Ge substrate (not shown here). For this reason, all TiO$_2$ films were deposited at substrate temperature of 450 °C after this experiment. Normally, to reduce the defect such as oxygen vacancy, annealing process is required. To investigate the interface reaction between TiO$_2$ and Ge during annealing process, XPS measurements was performed. Fig.3 shows Ge 3d spectra for the TiO$_2$/Ge stack structure. The GeO$_2$ formation was not observed at the TiO$_2$/Ge interfaces annealed at temperature below 300 °C in N$_2$ and O$_2$. However peak attributed to GeO$_2$ appeared for the TiO$_2$/Ge interface annealed at 500 °C in N$_2$, which means that GeO$_2$ was formed due to interface reaction between TiO$_2$ and Ge. This GeO$_2$ formation was supported by O 1s spectra.

Fig. 3 XPS spectra for TiO$_2$/Ge stack annealed in various conditions.

Electrical properties of a Pt/HfO$_2$/TiO$_2$/Ge MOS capacitor annealed at 300 °C in N$_2$ are shown in Fig. 4. The C-V characteristic of Pt/HfO$_2$/TiO$_2$/Ge MOS capacitor measured at 1 MHz (sweeping from inversion to accumulation) presented EOT = 0.84 nm estimated from the capacitance in the accumulation region and a small hysteresis, which is attributed to rutile TiO$_2$ interlayer. However, large flat band shift was also observed. It was reported that flat band shift voltages of TiO$_2$ is strongly related to structural defects and oxygen vacancy in TiO$_2$ film [11]. Therefore, changing deposition conditions of TiO$_2$ and PDA conditions enables to control flat band voltage. Current density is still high as shown in Fig. 4 (b), but acceptable to logic devices. High current density might be caused oxygen vacancy in HfO$_2$ and/or TiO$_2$. Yttrium doping into HfO$_2$ might lower the current density and moreover increase the dielectric constant of HfO$_2$ [12].

Fig. 4 Electrical properties of Pt/HfO$_2$/TiO$_2$/Ge MOS capacitor. (a) C-V characteristic and (b) I-V characteristic.

4. Conclusion

We tried to passivate the Ge surface using the rutile TiO$_2$ interlayer to enhance the electrical properties of the high-k/Ge MOS structure. The rutile TiO$_2$ interlayer achieved lower EOT = 0.84 and small hysteresis in the C-V characteristic. However, large flat band shift was also observed, which can be controlled by deposition conditions of TiO$_2$ and PDA conditions. Therefore, the rutile TiO$_2$ interlayer is promising method to passivate Ge surface for Ge MOS devices.

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Reference