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Suppression of short channel effects in accumulation-type UTB-InGaAs-OI nMISFETs with raised S/D fabricated by gate-last process

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Abstract

Accumulation-type (junction-less) 8-nm thick UTB-InGaAsOI nMISFETs with raised SD were fabricated by gate-last process. It was confirmed that the raised SD structure drastically reduced parasitic resistance at the SD regions. It was found that the short channel effects were comparable to those of gate-all-around FETs below L_g < 100 nm even with In content of 70%.

1. Introduction

An ultra-thin body (UTB) III-V on-Insulator nMISFET on a Si substrate is one of the promising structures. This structure enables Si compatible process except for the lower thermal budget. It can also make it possible to suppress the short channel effects (SCEs) comparably with non-planar FETs such as FinFETs or gate-all-around (GAA) FETs with simpler planar processes [1-3]. UTB-InGaAs-OI nMSIFETs with raised n^+-InGaAs SD structures have been demonstrated [4]. However, the parasitic resistance was still high [3] because of the offset below the gate-sidewall in the devices. In order to reduce the parasitic resistance, a gate-last process with raised SD without the offset regions is preferable. Furthermore, the gate-last process makes it possible to choose gate-stacks such as TaN/Al_2O_3, of which thermal stability are not sufficiently high, but which can provide proper V_{th}, high mobility and low interface states density [5]. On the other hand, an accumulation-type or a depletion-type (junction-less) FET is attractive since lower parasitic resistance can be expected without complicated extension formation processes. Junction-less FETs are also expected to show higher mobility than those of inversion-type [6]. However, the short-channel effects (SCEs) are one of concerns of accumulation-type transistors. In this study, 8-nm-thick InGaAs-OI accumulation-type nMISFETs with raised SD fabricated by a gate-last process are demonstrated. SCEs were examined by evaluating gate-length dependences of SS and Vth.

2. Experimental

The process flow of the UTB-InGaAs-OI nMISFET is shown in Fig. 1. Si-doped ($N_D = 1 \times 10^{18}$ cm^{-3}) 10-nm-thick $In_xGa_{1-x}As$ (x= 0.53, 0.7) channel layers were grown on (001) p-InP substrates by MOCVD. 20-nm-thick Al_2O_3 layer as a buried oxide layer was deposited on the InGaAs/InP substrates. The Al_2O_3 / InGaAs / InP substrates were bonded to Si substrates in vacuum after ion beam activation of Si substrates' surfaces, followed by etching of the InP supporting substrates using HCl aqueous solution [7]. SiO_2 dummy gates with L_g of down to 70 nm were formed on the InGaAs-OI substrates. n^+-InGaAs layer with thickness of about ~40 nm was then epitaxially grown by MOCVD. Next, InGaAs active areas were formed by mesa-isolation after removing the SiO_2 dummy gates. The wafers were dipped in $(NH_4)_2Se$ solution for 2 min to improve MOS interface quality [8] and successively loaded into an ALD chamber. Al_2O_3 of 75cycle (~8 nm) for $In_{0.53}Ga_{0.47}As$ and Al_2O_3 of 40cycle (~ 4 nm) for $In_{0.7}Ga_{0.3}As$ were deposited. Then, TaN 20 nm, a-Si 10 nm was sputtered. Just after gate electrode deposition, PMA was done at 350 ^oC for 10 min in N_2 atmosphere, followed by gate patterning. Contact pads of 100-nm Au/10-nm Ti bilayer were formed on the n^+-InGaAs SD regions by a lift-off process. Device fabrications were finished with 2nd PMA at 300 ^oC for 10 min.

3. Results

Fig. 2 shows SEM images of epitaxial n^+-InGaAs layers on the InGaAs-OI substrates (initial T_{body} = 10 nm) grown at 540 ^oC and 565 ^oC. A summary of mobility, carrier concentration (N_D), and sheet resistance (R_{sh}) of epitaxial n^+-InGaAs layers grown at various temperatures, which were evaluated by Hall measurements, is also shown. Epitaxial growth at and above 565 ^oC caused agglomeration of InGaAs layer resulting from decreasing surface free energy, which often occurs also in UTB-SOI substrate after high temperature anneal [9]. On the other hand, 520 ^oC epitaxial growth resulted in significantly high sheet resistance because of the low carrier concentration and the low mobility. In this study, 540 ^oC was set for the epitaxial growth temperature, which is smaller than that of n^+InGaAs on a bulk substrate [4]. Fig. 3 shows a cross sectional TEM image of the $In_{0.53}Ga_{0.47}As$ nMISFET with L_g = 70 nm. It shows the n^+InGaAs layer was grown without agglomeration and defects. Fig. 4 shows the gate length dependence of on-resistance, R_{on}. The large parasitic resistance of the devices without the raised SD is probably due to the surface depletion of UTB S/D. It is shown that raised S/D drastically reduced on-resistance. However, the constant R_{on} dependency on L_g suggests that it is still limited by the parasitic resistance. I_d-V_g characteristics of $In_{0.7}Ga_{0.3}As$-OI nMISFET with L_g = 115 nm are shown in Fig. 5. I_d-V_g characteristics of inversion-type device are also shown as a reference. It was found that the both type of devices exhibits similar sub-threshold characteristics, indicating no degradation of SCEs in the accumulation-type device due to such a thin body of 8 nm. Fig. 6 shows I_d-V_d characteristic of the $In_{0.7}Ga_{0.3}As$ nMISFET. Saturation characteristics and I_{on} = 310 uA/um at V_{dd} = 1 V and V_g = 3 V were obtained. The I_{on} value is about one order of magnitude higher than in [4] thanks to the device structure without the offset regions. Further performance enhancement would be expected by reducing the parasitic resistance. Figs. 7 and 8 show L_g dependence of SS and V_{th} shift for the $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$-OI MISFETs. These figures indicate that SCEs controllability is comparable to that of GAA [10] due to the thin body of 8nm even with In content of 70%.

3. Conclusions

We have demonstrated accumulation-type (junction-less) 8-nm thick UTB-InGaAsOI nMISFETs with raised SD fabricated by gate-last process. It was confirmed that the raised SD structure drastically reduced parasitic resistance at the SD regions. It was found that the short channel effects were comparable to those of GAA FETs below L_g =130 nm with In content of 70% due to the sufficiently thin channel layer.

Acknowledgements

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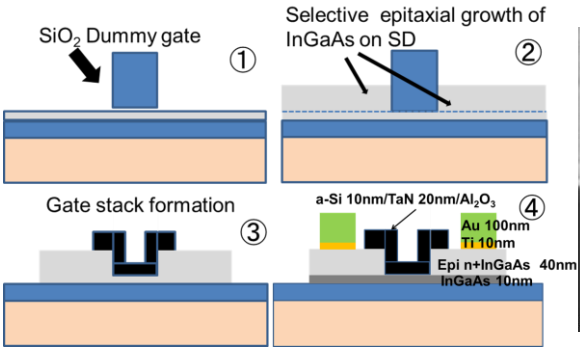
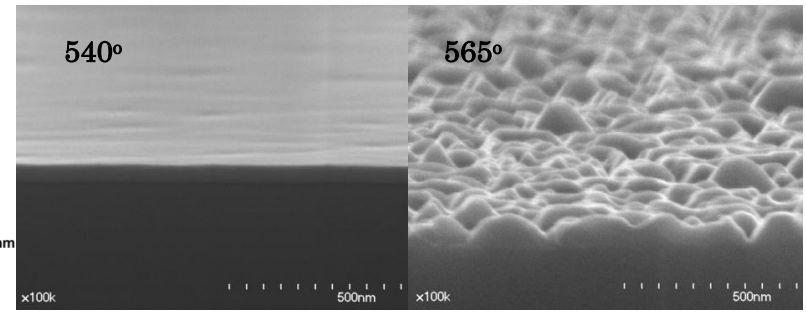


Fig. 1 Schematic of gate-last fabrication procedure of UTB–InGaAs-OI nMISFETs with raised SD of n^+InGaAs.



	Mobility (cm^2/Vs)	Rsh (Ω/□)	Nd (cm^{-3})
520 °C	330	1400	1.0E+17
540 °C	1100	35	1.5E+19
565 °C	Agglomeration		
580 °C	Agglomeration		

Fig. 2 SEM pictures of n^+InGaAs layers grown at 540 and 565°C on UTB InGaAs-OI substrates. Summary of mobility, sheet resistance R_{sh}, and carrier concentration N_d for each epitaxial growth condition are also shown.

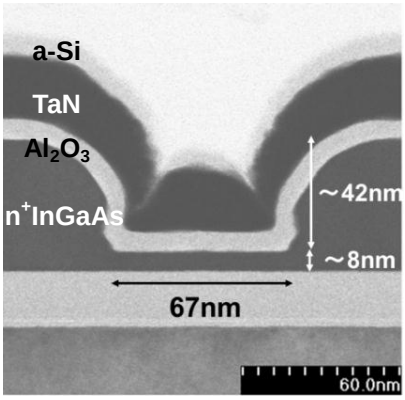


Fig. 3 Cross sectional TEM image of $In_{0.53}Ga_{0.47}As$-OI nMISFET with the gate length of about 70 nm.

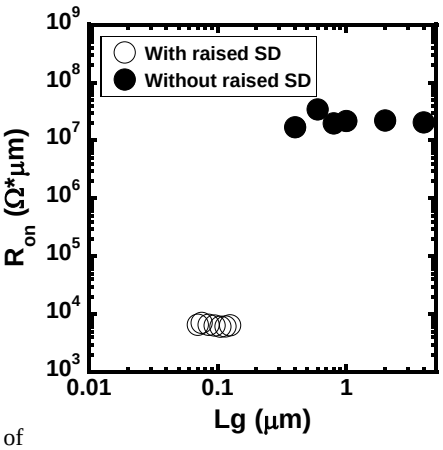


Fig. 4 R_{on}-L_g plot of $In_{0.53}Ga_{0.47}As$-OI nMISFETs with and without raised SD. R_{on} is defined as V_d/I_d at V_d = 0.05V, V_g-V_t = 1V.

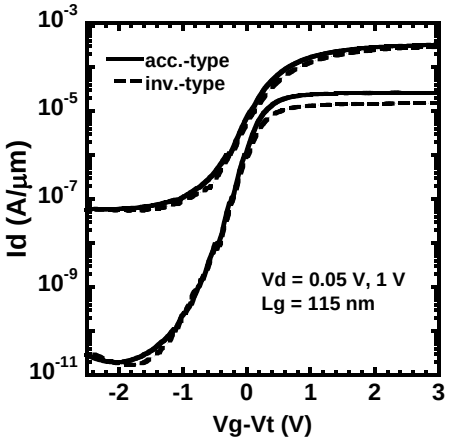


Fig. 5 I_d-V_g characteristics of $In_{0.7}Ga_{0.3}As$–OI nMISFET with L_g =115nm. I_d-V_g characteristics of inversion-type $In_{0.7}Ga_{0.3}As$–OI nMISFET are also shown as a reference.

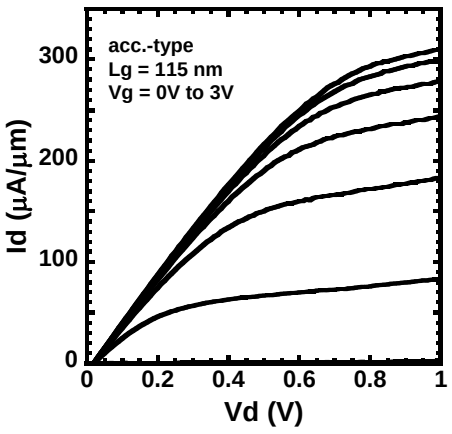


Fig. 6 I_d-V_d characteristics of $In_{0.7}Ga_{0.3}As$–OI nMISFETs with L_g =115 nm.

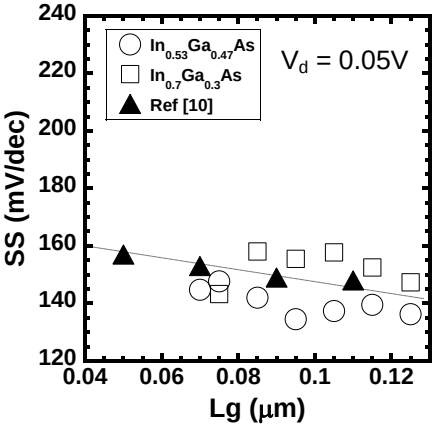


Fig. 7 L_g dependence of SS at V_d = 0.05 V for $In_{0.53}Ga_{0.47}As$- and $In_{0.7}Ga_{0.3}As$-OI nMISFETs. SS is comparable to that of GAA [10] below L_g < 130nm. In this work, Al_2O_3 thickness is about 8nm for $In_{0.53}Ga_{0.47}As$, 4nm for $In_{0.7}Ga_{0.3}As$ and that of Ref. [10] is 10nm.

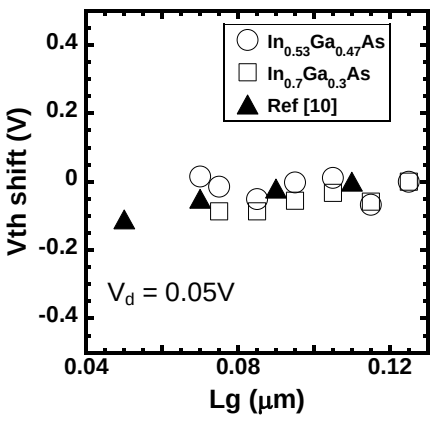


Fig. 8 L_g dependence of ΔV_{th} from V_{th} of L_g = 125 nm for $In_{0.53}Ga_{0.47}As$- and $In_{0.7}Ga_{0.3}As$-OI nMISFETs. ΔV_{th} from V_{th} of L_g = 110 nm of Ref. [10] is also shown. Distinct V_{th} roll-off is not observed.