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Current-Mode Ambient Light Sensor for Ultra Low Power Applications

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Abstract

A novel ambient light sensor with progressive sizing current mirrors for analog-to-digital conversion is proposed. By successive approximation register logic, adjustable dynamic range is obtained for ambient light sensing. This new design operates well under low supply voltage (<1V) for meeting the ultra low power requirement in distributed sensor node applications.

1. Introduction

Low power and low cost ambient light sensors allows for the collection a large amount of environmental data in a vast region for smart electronic systems[1]. Combining various sensors on a chip, one can construct a low cost environmental sensing modules that run on limited power, such as, from solar panels or other energy harvesting devices [2]. The distributed sensor systems provide instant updates on the environmental changes, with minimal maintenance. Commercial products capable of wide detection range (1~10000 lux) is generally too large in size and requires high power, making them unsuitable for integrated sensor chips. In this paper, a self-correlated light detection solution is presented. The current-mode mirroring circuits enables photo-sensing signal to be converting to digital data through binary successive approximation logic. As a result, a low power (2μJ/data) low driving voltage (1V) and 6 bits digital output solution is presented.

2. Photodiode characteristics

The inset of Figure 1 illustrates the 3T APS circuit designed to extract the characteristics of a n+/p-well photo-diode (5×5μm^2) in 0.18-μm 1P6M CMOS logic process. The photo-response is measured under a 3200K tungsten-halogen lamp and integration sphere for uniform source of illumination. Figure 1 shows its output signal drop during an integration period for the extraction of the photo-current. The extracted photo-current fitted by simulation data is shown in Figure 2, where the quantum efficiency is found to be 15%. A dark current level of 3.6fA under 1.8V is extracted by measurement data as well.

3. Operation scheme

Block diagram in Figure 3 illustrates the basic operation of the low power ambient light sensor. First, the incident light is converted into photo-current, I_{ph}, and then transformed into voltage ramps by a detector circuit. This upward ramp, V_o, is then fed into a comparator producing a pulse indicating intersecting point when $V_O=V_{ref}$. The pulse signal compared with a clock signal results in a binary signal which controls the successive approximation register (SAR).[2] The SAR code evolves successively to decode the photocurrent level by feeding M back to the detector circuit. Figure 4 illustrates the schematic of the detector circuit composed of a photodiode, current mirrors [3], and a capacitive load. The current mirrors with weighted ratio are controlled by the digital code output from the SAR logic circuit. The sum of the weighted photocurrent, $M*I_{ph}$, charging up C_L, produces V_O with a ramp rate proportional to $M*I_{ph}$. The charging current vs. I_{ph} in Figure 5 reflects a fairly linear response I_{ph} > 50fA, with less than 2% error in resulting current ratio. V_O, is transformed to pulse width, ΔT, by a comparison with V_{ref}. Figure 6 shows the relationship between the ambient light intensity and 1/ΔT.

4. Results and Discussions

If ΔT ended before the clock's positive edge, then output stage output is "1", otherwise is "0", as illustrated in Figure 7. By controlling the select transistors by SAR output (M), binary successive approximation algorithm completes I_{ph}-to-M conversion after 6 successive cycles, as illustrated in Figure 8. For ambient light sensing, we assume that light intensity remains the same during a sensing cycle of 1 second. In Figure 9, the digital output proportional to ΔT, is inversely proportional light intensity. The impact of transistors' V_{th} and width variations on the ΔT is investigate by Monte Carlo simulation. V_{th} and W distributions is based on the mathematical models reported in [4]. The circuit is most susceptible to V_{th} variation, however, data suggested it only causes less than 1% error. It is found that the majority power lost in the static leakage power in SAR logic and comparator circuits, while the transient power is negligible. As reveals in Figure 11, V_{DD} scaling can effectively reduces power by 80%. For low-speed applications, V_{DD} is set to 1V to obtain a low power consumption of 5μW. By increasing the channel length of transistors also achieves power saving with significant area penalty. Minimum transistor length of 0.5μm is chosen, for obtain an running power of 2μW without suffer too much in chip area. Table 1 compares the performance level of this new ambient light sensor and that reported in [5]. Much smaller circuit as well as lower power consumption is achieved.

5. Conclusions

In this work, a novel ambient light sensor with correlative photo-current mirrors to improve its power consumption and with pulse width comparison algorithm to achieve adjustable dynamic range is proposed. Simulation results suggest that a low power ambient sensing with digital output is demonstrated.

Reference

[1] Akyildiz, I.F. et al , Computer Networks, Vol. 38, Number 4,15, pp. 393-422(30), 2002
[2] Warneke, B.A. et al, IEEE-sensors, vol.2, p. 1510 - 1515 2002
[3] Shaker, M.O. et al., IEEE-ISQED, p. 1 -5, 2011
[4] Cho, S.-I. et al l., IEEE-EL,vol.47,pp. 981 – 983, 2011
[5] Maxim, A. et al., IEEE-ISCAS, vol.5, p. 511 – 514, 2001

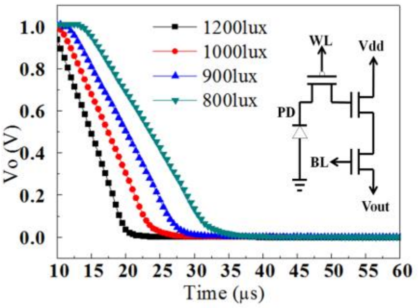

Figure 1 Photo-response of the 3T APS for photo-current extraction of PD.

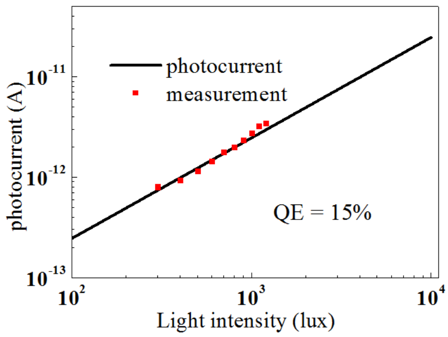

Figure 2 Photodiode's quantum efficiency and dark current extraction by simulation fit.

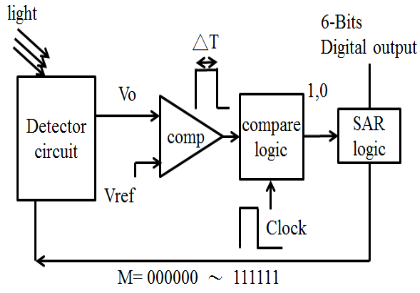

Figure 3 Block diagram of the digital output ambient light sensor circuit.

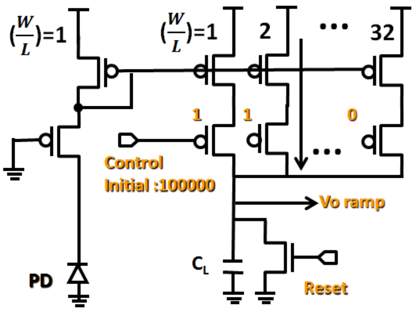

Figure 4 Schematic of the photo-detector circuit producing a voltage ramp.

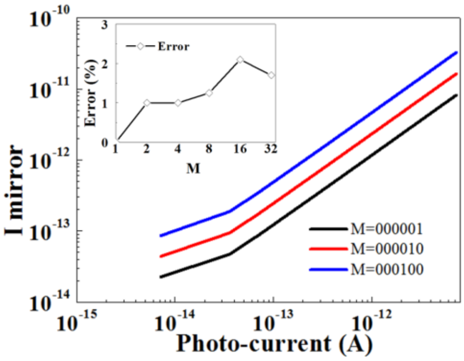

Figure 5 Mirrored current vs. Iph. Its lower bound limits the minimal detection level.

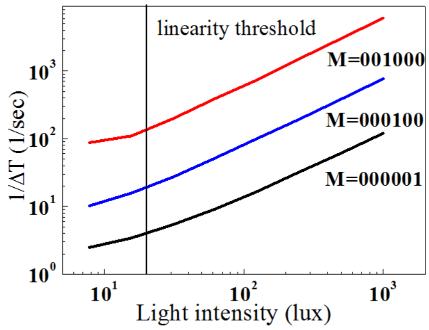

Figure 6 Pulse width vs. light intensity shows monotonically increasing characteristics.

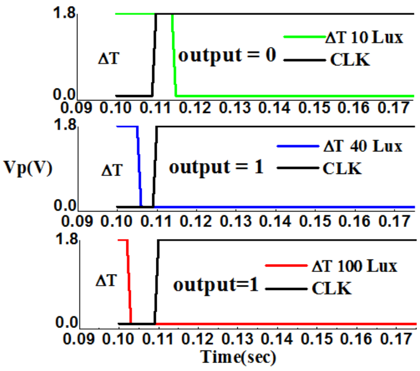

Figure 7 Input and output signals of the compare logic circuit at various light intensities.

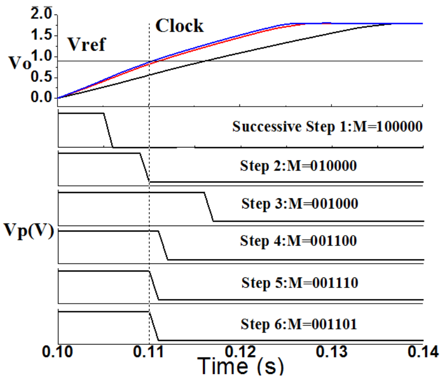

Figure 8 A illustration example of the success approximation steps.

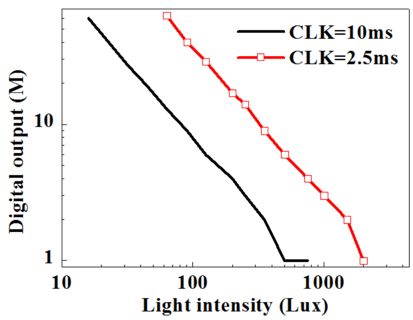

Figure 9 Digital output vs. light intensity at different clock rates resulting change in its sensing ranges.

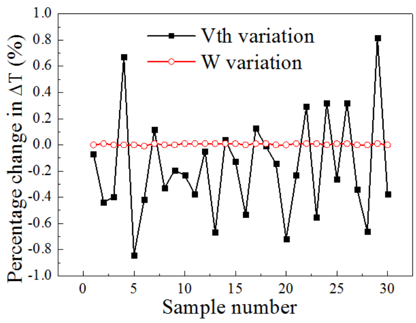

Figure 10 Monte-Carlo simulation results when considering V_{th} and W variations.

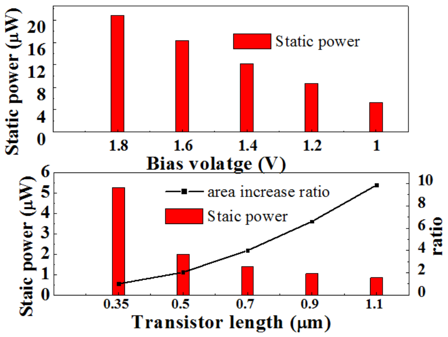

Figure 11 Power reduction methods by V_{DD} scaling and increasing channel length.

	This work	Ref[5]
Sensor type	Digital	Digital
Dynamic Range	18dB	20dB
Resolution	6Bits	5Bits
Integration time	1s	300ms
Internal clock frequency	100Hz	107Hz
Light perceiving area	5μm by 5μm	650μm by 450μm
Power consumption (at 1000 LUX worst case for SAR)	2uJ/cycle I_{av}=2μA	I_{av}=5μA
Supply voltage	1.8~1.0V	5V
Technology	Standard CMOS 0.18μm	Standard CMOS 0.5μm

Table 2. Performance comparison of this work vs. that reported in [5]