Study of Trap Properties of High-k/Metal Gate pMOSFETs with Aluminum Ion Implantation by Random Telegraph Noise and 1/f Noise Measurements

Tsung-Hsien Kao¹, Sun-Lein Wu², Kai-Shiang Tsai², Yean-Kuen Fang¹, Bo-Chin Wang¹, Chien-Ming Lai¹, Chia-Wei Hsu³, Yi-Wen Chen³, Osbert Cheng¹ and Shou-Jinn Chang²

¹ Institute of Microelectronics and Department of Electrical Engineering, Advanced Optoelectronic Technology Center, Center for Micro/Nano Science and Technology, National Cheng Kung University, Tainan City 701, Taiwan
² Departments of Electronic Engineering, Cheng Shiu University, Kaohsiung City 833, Taiwan
³ Central R&D Division, United Microelectronics Corp. (UMC), Tainan City 744, Taiwan

Phone: +886-6-2757575 ext. 62391 Fax: +886-6-2671854 * e-mail: q18011247@mail.ncku.edu.tw

1. Introduction

At the 45-nm technology node and beyond, high-permittivity (HK) materials and metal gate (MG) electrodes have extensively replaced conventional SiO₂ gate oxide and poly-gate, respectively, to solve such problems as poly-gate depletion, gate sheet resistance, boron penetration, and Fermi level pinning. However, fabricating a metal gate p-type metal-oxide-semiconductor (PMOS) transistor with low threshold voltage (V_th), especially with a small equivalent oxide thickness (EOT), is crucial in gate-first integration owing to the presence of various oxygen vacancies and defect sites in the HK gate dielectric. Recently, to obtain large VSB shift with minimized EOT penalty in HK/MG pMOSFETs, aluminum (Al) ion implantation (II) technology was implemented and identified as an effective approach for effective work function (EWF) modulation in PMOS [1] without ETO increasing and complicated process. On the other hand, the low frequency noises including 1/f noise and random telegraph noise (RTN) which is attributed to the random trapping/detrapping process of signal or multiple traps in the gate dielectric have attracted considerable attention as the most appropriate approaches to analyzing the traps in the HK/MG devices. Especially, the analysis on RTN in HK/MG stacks devices to determine whether an oxide trap leading to RTN is located in high-k layer or in interfacial layer (IL) and then to characterize such a trap will be beneficial to develop new process flow evolution. In this paper, we present the correlation between RTN and 1/f noise parameters in HK/MG stacks pMOSFETs with aluminum (Al) ion implantation (II).

2. Device Structure and Experiment

For this work, all pMOSFET devices were fabricated using 28 nm high-k/metal gate (HK/MG) technology. The gate dielectrics consist of a 1-nm thermal-grown SiO₂ as an interfacial layer (IL), followed by a 2 nm atomic layer deposition HfO₂ HK film. A 10-nm radio-frequency PVD TiN was deposited as gate metal, then HK/MG samples were performed by Al ion implantation through TiN layer at 1.2 keV with dose of 5 × 10¹⁰ cm⁻² (referred to device A) and 1 × 10¹⁰ cm⁻² (referred to device B) respectively. For comparison, HK/MG pMOSFETs without Al II were also fabricated and labeled as control device. Prior to noise measurements, the dc characteristics were measured using an Agilent B1500 Semiconductor Parameter Analyzer. The 1/f noise measurements were carried out using SR570 low-noise current preamplifiers and Agilent 35670A dynamic signal analyzer. The pMOSFETs were biased in linear operation (VPD = -50 mV) while varying the gate overdrive voltage (VG - VT) from the subthreshold regime (0.2 V) to the strong inversion regime (-0.5 V). The random telegraph noise (RTN) measurements were made by waveform generator/fast measurement unit modules based on Agilent B1500 semiconductor parameter analyzer.

3. Results and Discussion

Fig. 1 shows the drain current (ID) as a function of drain voltage (V_D) for all HK/MG pMOSFETs. Around 7% and 13% and 7% is enhancement obtained for device A and B, respectively. As compared to the control at a fixed gate overdrive, VG - VT = -0.8 V, and VD = -1.0 V. The threshold voltages (VT) for device A, B, and the control are -0.55 V, -0.46 V, and -0.73 V, respectively. The results indicated that Al implanted through TiN metal leads the EWF closer to the Si valence band edge, which was ascribed to the interface-dipole layer involving Al oxide formed at the HfO₂/SiO₂ interface. To investigate the impact of Al I/I on 1/f noise of HK/MG devices, the normalized drain current noise spectral density SD for all samples taken from the average of six devices biased at different gate overdrive voltages is presented as Fig. 2. All devices show typical 1/f noise type with the frequency exponent close to unity for all gate overdrives. The noise level in devices A and B is observed to be significantly lower than the control with no Al implant, which implies high-k layer has lower trap density. The normalized drain current noise spectral density (SD / ID) and the transconductance to drain current squared (g_m / ID) as a function of drain current is plotted in Fig.3 to confirm the physical mechanism of 1/f noise. The LS_D / ID was extracted at f = 25 Hz for all devices. The LS_D / ID² curve of all devices shows cannot follow this trend at high current with (g_m / ID)², which implies that either of the correlated mobility fluctuation (AM) or source/drain (S/D) series resistance is major noise mechanism and need to be clearly clarified [2]. Using Fig 4, all devices shows (V_D - V_T)⁰.⁵ with m = 0.98, which highlights that the S/D noise can be excluded from overall noise. In order to further evaluate the parameters of 1/f noise model on all devices, the normalized input-referred voltage noise spectral density (LS_V) as a function of the V_D - V_T is shown in Fig. 5. As expected, all devices show two distinct regions in the associated LS_V. In region I (V_G - V_T < 0.2 V), the LS_V is independent of V_G - V_T, which indicate a signature of umber fluctuations. In region II (V_G - V_T > 0.2 V), a pronounced LS_VO dependence on V_G - V_T indeed proves that correlated mobility fluctuations was involved. Fig. 6 shows the time domain drain current RTN fluctuations (I_D-RTN) at various gate voltages for all HK/MG devices. A distinct difference in drain current between two states was observed, which are responsible for carrier trapping and detrapping at a single trap site. The extracted mean capture time (τ_c) and mean emission time constant (τ_e) versus gate overdrive (V_G - V_T) are presented in Fig. 7. The lower values of τ_e for both devices A and B with Al I/I technique indicate that the capture probability of carrier becomes larger. The value of dln(τ_c)/dV_G, time constant variation rate, will determine whether a trap is located in the high-k dielectric or the SiO₂ IL after Al I/I experiment. Fig. 8 shows the dependence of the ln(τ_e/τ_c) with respect to the V_G - V_T for all devices. The dashed lines represent linear fitting curve to extract the trap depth (x_t), away from the SiO₂ /LSi interface, using the conventional method [3]. Interestingly, the trap position x_t will shift from 2.59 nm...
for the control to 2.22 nm (1.95 nm) for device A (B) with Al ion implantation. Although the trap for all devices is located in the high-k material layer, device B is closer to the SiO2/IL/Si interface. The smaller xi implies the reduction tunneling attenuation length (λ), which is an important parameter in 1/f noise. The relation between xi and λ can be express as [4]

\[ x_i = A \cdot \ln \left( \frac{1}{2\pi f \tau_0} \right) \]

where the time constant τ0 is often taken as 10−10 s. The λ values for hole tunneling at a f = 25 Hz were calculated as 1.65 × 10−3, 1.42 × 10−3, and 1.24 × 10−3 cm for the control, device A, and B, respectively. Due to the LSVG in region I, as shown in Fig. 5, is proportional to λN0 [5]. Applying the calculated λ values to the data in Fig. 5, we found that the extracted trap density Nt were 2.79 × 1019, 1.07 × 1019, and 8.01 × 1018 cm−3 eV−1 for the control, device A, and B, respectively. Although the interfacial Al2O3 layer was formed at the the HfO2/SiO2 interface, we found that employing Al ion implantation in HK/MG devices has little influence on trap density. Therefore, the implantation energy and dose to obtain Al distribution profile shifted toward HfO2/SiO2 interface without degradation in reliability performance should be well controlled by the optimized process.

3. Conclusions

We have investigated the trap behavior in pMOSFETs with different concentrations of Al implant in high-k dielectrics by using 1/f noise and RTN measurements simultaneously. Compared with the control device, device A and B with considerably lower 1/f noise level was observed, which is resulting from the decrease in λ and N0. The xi of devices B closer to SiO2/IL/Si interface maybe resulted from that Al distribution profile shifted more toward HfO2/SiO2 interface.

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References