Abstract

Impacts of high-mobility channels on footprints of a CMOS circuit were examined. Under a condition of fixed $V_{TH}$ variation and operation speed, it was revealed that high-mobility channels are effective to reduce channel width without increasing $V_{TH}$ variation. An area of a 256kbit SRAM of 65 nm technology was estimated to be reduced to 77% by placing Si/n/pMOSFETs with In$_{0.53}$Ga$_{0.47}$As/Ge-channel MOSFETs.

1. Introduction

The trend toward miniaturization of CMOS devices has resulted in lowering power supply voltage, which is expected to be less than 1 V within a few years. In order to realize high operation speed with such low power supply voltage, devices having a high-mobility-channel MOSFETs made of new materials such as Ge, SiGe, and III-V semiconductors are being intensively investigated [1, 2]. As miniaturization continues, wire delay increases while intrinsic delay decreases [3]. Hence it is considered that $V_{DD}$, which is defined by $\Delta V_{TH}$, is still important as an index of operation speed even in digital circuits. Here, $J_D$ is drain current which is not divided by channel width and $V_G$ is gate voltage. It is expected that high-mobility-channel devices make it possible to design device width narrowed and/or channel length longer than in Si-channel devices, without reducing $J_D$. The former possibility results in reducing device area and suppression of $V_{TH}$ variation is required. In this study, we quantitatively investigated relationships between device width, which has a great impact on a circuit footprint, and $V_{TH}$ variation in planar Si-Ge and In$_{0.53}$Ga$_{0.47}$As-on-insulator MOSFETs under a condition of fixed Gm using device simulations.

2. Procedure of Device Simulations

Current-voltage characteristics for planar MOSFETs with a micromachined-insulator structure were calculated using a device simulator HyNEEXSTM [4]. Simulation parameters of the mobility model as a function of the transverse electric field were adjusted to reconstruct observed relationships between effective mobility and effective field for Si-Ge [5], Ge-He [6-8], and In$_{0.53}$Ga$_{0.47}$As [8] MOSFETs on (001) surface. A drift-diffusion model was used in the simulations. In order to take velocity overshoot into consideration effectively, parameters that are related to saturation velocity were adjusted so that the injection velocity is the Si one multiplied by a factor of (mobility/Si mobility)$^{0.43}$ [10]. Here, injection velocity was estimated by calculating ratio of drain current to inversion charge density, which was calculated by integrating gate capacitance over gate voltage. Device structure is schematically shown in Fig. 1. Firstly, $g_m$, which is defined by $\frac{\partial I_D}{\partial V_G}$, was calculated by dividing a required value for Gm by $g_m$. Here, a required value for Gm in the case of that $V_{DD} = 1$ V was set to 1 mS, for instance. As it is written later, qualitatively equivalent results are obtained even for other values for Gm. Thirdly, $V_{TH}$ variation ($\Delta V_{TH}$) was calculated. In this study, only $\Delta V_{TH}$ due to Line Edge Roughness (LER) was taken into consideration for simplicity, because $\Delta V_{TH}$ due to Random Dopant Fluctuation (RDF) is estimated to be smaller than that due to the LER by more than 1 order of magnitude because of the low impurity concentration in the channel region (Fig. 1). As for $\Delta V_{TH}$ due to variation of channel layer thickness ($\Delta T_{CH}$), it is assumed in this study to be reasonable because correlation length of $\Delta T_{CH}$ is considered to be much longer than $L_G$. $\Delta V_{TH}$ due to the LER is modeled by $\Delta V_{TH} = (\delta V_{TH}/\delta L_G) \times (W_C/W)\times\Delta L_G$, where $W_C$ is a correlation length of the LER and $\Delta L_G$ is a $L_G$ variation due to the LER [11]. Reported values of $W_C = 25$nm and $\Delta L_G$ (3 x standard deviation) = 5 nm [12] were used in this study. Fourthly, $\Delta V_{TH}$-W relationships were compared among the Si-, Ge-, and In$_{0.53}$Ga$_{0.47}$As-channel MOSFETs. Finally, reduction in a region of a 256kbit SRAM circuit of 65 nm technology was estimated as an instance.

3. Results and Discussion

Firstly, $g_m$-$V_G$ characteristics were calculated for the Si-, Ge-, and In$_{0.53}$Ga$_{0.47}$As-channel nMOSFETs having a $L_G$ of 20 to 100 nm. (Fig. 2) Because $g_m$ depends on $V_G$, only maximum values of $g_m$ ($g_m$-max) were considered in this study. (Fig. 3) Secondly, $W$ was calculated for the Si-, Ge-, and In$_{0.53}$Ga$_{0.47}$As-channel nMOSFETs. (Fig. 4) $W$ of the Ge/In$_{0.53}$Ga$_{0.47}$As-channel nMOSFETs with $L_G = 30$ nm, for instance, are reduced to 69/31% of the Si nMOSFET because of the high mobility. Thirdly, using $\Delta V_{TH}/\delta L_G$ (Fig. 5), $\Delta V_{TH}$ was plotted as a function of $W$. (Fig. 7) For instance, $W$ of the Ge/In$_{0.53}$Ga$_{0.47}$As-channel nMOSFETs are calculated to be 70/31% of that of the Si nMOSFET for $\Delta V_{TH} = 5$ mV. Same procedure was carried out for Si- and Ge-channel pMOSFETs. (Fig. 8) For $\Delta V_{TH} = 5$ mV, for instance, W of the Ge-channel pMOSFET is reduced to 57% of that of the Si pMOSFET. $L_G$ and W of these devices are summarized in Table I. Although only cases for specific values of Gm, $W_C$, and $\Delta L_G$ were studied above, qualitatively equivalent results are obtained even for other values of Gm, $W_C$, and $\Delta L_G$. Because, in case Gm, $W_C$, and $\Delta L_G$ are multiplied by A, B, and C, respectively, which are arbitrary positive constants, $W$ and $\Delta V_{TH}$ is multiplied by A and (B/A)$^{1/2}$ x C, respectively. Therefore, it is concluded that high-mobility-channel MOSFETs have an advantage in reducing device width under a condition of fixed Gm using device simulations. 256kbit SRAM circuit area of 65 nm technology were estimated assuming that only the peripheral circuit, which covers 60% of the total circuit area [13], was shrunk and that cell areas are kept constant. Equal number of p- and nMOSFETs and STI spacing of 290

nm were also assumed. The chip area is estimated to be reduced to 77% by replacing Si n/p MOSFETs to In0.53Ga0.47As/Ge-channel MOSFETs under a condition of $\Delta V_{TH} = 5$ mV and $Gm = 1$ mS.

4. Conclusion

It has been shown that device width can be reduced under a condition of a fixed $V_{TH}$ variation and $Gm$ for high-mobility channel MOSFETs. Hence, chip area is reduced under a condition of a fixed $V_{TH}$ variation and $Gm$ by adopting high-mobility channel MOSFETs, for instance Ge and In0.53Ge0.47As. 256kbit SRAM circuit areas, for instance, were estimated to be reduced to 77% by replacing Si CMOS circuit to In0.53Ga0.47As/Ge hybrid one.

Acknowledgment

The authors are grateful to Dr. K. Fukuda of National Institute of Advanced Industrial Science and Technology and Dr. T. Ohguro of Toshiba Corporation for their useful comments. This research is granted by the Japan Society for the Promotion of Science (JSPS) through the “Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program),” initiated by the Council for Science and Technology Policy (CSTP).

References


Fig. 1. Device structure that is used in this study.

Fig. 2. gm-$V_D$ characteristics for nMOSFETs. Here, $L_G = 30$ nm and $V_D = 1$ V.

Fig. 3. Dependences of maximum values of gm ($gm_{max}$) on $L_G$ for nMOSFETs. Here, $V_D = 1$ V.

Fig. 4. Dependences of device widths (W) for realizing $Gm = 1$ mS on $L_G$ for nMOSFETs. Here, $V_D = 1$ V.

Fig. 5. Dependences of $\Delta V_{TH}/L_G$ on $L_G$ for nMOSFETs. Here, $V_D = 1$ V.

Fig. 6. Dependences of $V_{TH}$ variation ($\Delta V_{TH}$) on $L_G$ for nMOSFETs. Here, $V_D = 1$ V.

$\Delta V_{TH} = 5$ mV

Table I. $L_G$ and W for realization of $Gm = 1$ mS. Here, $V_{DD} = 1$ V and $\Delta V_{TH} = 5$ mV.